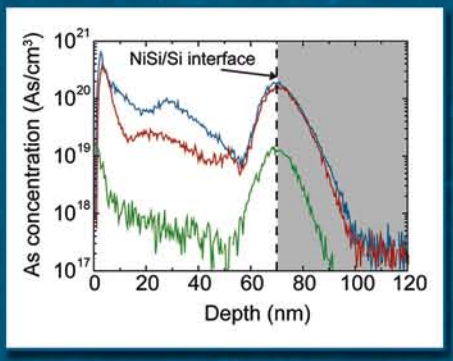

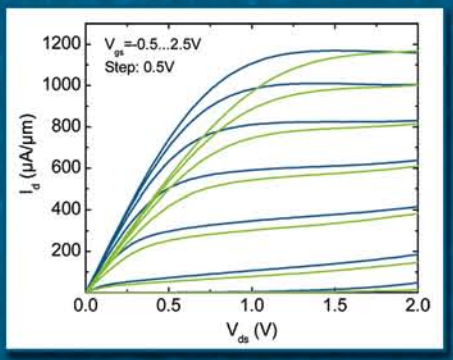

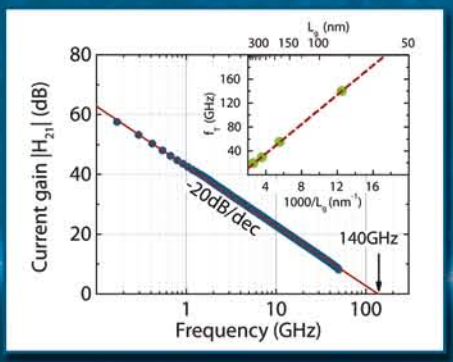

DC and RF Characterization of NiSi Schottky Barrier MOSFETs with Dopant Segregation

Christoph Johannes Urban

Mitglied der Helmholtz-Gemeinschaft

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Kurzfassung

Die fortschreitende Skalierung der Silizium-basierten Mikroelektronik, welche die Basis der heutigen Informationsgesellschaft bildet, bedarf neuer Konzepte für die Source-Drain (S/D) Kontakte der Metall-Oxid-Halbleiter Feldeffekttransistoren (MOSFET). Dabei ist insbesondere eine Verbesserung der Ladungsträgerinjektion wichtig, da der zunehmende Einfluss der parasitären Widerstände die Leistungsfähigkeit von hochgradig skalierten Bauelementen stark begrenzt. Darüber hinaus werden immer abruptere Übergänge zwischen Kontakt und Kanal für Bauelemente auf der Nanometerskala erforderlich. In diesem Zusammenhang sind Schottky-Barrieren (SB) MOSFETs mit metallischen S/D Kontakten sehr vielversprechend, da sich mit ihnen niedrige extrinsische Widerstände und atomar abrupte Kontakt-Kanal-Übergänge an den Metall-Silizium Grenzflächen realisieren lassen. Ein großer Nachteil ist jedoch, dass die Leistungsfähigkeit dieser Bauelemente der von konventionellen MOSFETs aufgrund der relativ hohen Schottky-Barriere unterlegen ist. Kürzlich erregte die sogenannte Dotierstoffsegregation großes Interesse, da die bei der Silizidierung entstandene hochdotierte Schicht an der Silizid-Silizium Grenzfläche die Tunnel-Wahrscheinlichkeit von Ladungsträgern durch Schottky-Kontakte stark erhöht.

Die vorliegende Arbeit untersucht experimentell die Integration von NiSi mit Dotierstoffsegregation für den Einsatz in SB-MOSFETs auf dünnem Silizium-auf-Isolator (SOI). Ziel der detaillierten Gleichstrom (DC) und Hochfrequenz (RF) Charakterisierung ist der Erhalt eines besseren Einblickes in die Physik dieser Bauelemente.

Die Modellierung von NiSi/p-Si Schottky-Kontakten mit Hilfe eines numerischen Modelles, welches die Thermische-Emissions-Theorie mit der Barrierenverkleinerung durch Spiegelladungen und quantenmechanischem Tunneln kombiniert, vertieft das Verständnis der Ladungsträgerinjektion von Schottky-Kontakten. Schottky-Dioden mit Dotierstoffsegregation von Bor, Arsen und Antimon, die durch die Silizidierung herbeigeführt wurde, zeigen abhängig von der Implantationsdosis effektive Schottky-Barrieren-Höhen um 0.1 eV. Unterhalb dieses Wertes sind SB-MOSFETs in der Lage die Leistungsfähigkeit von konventionellen Bauelementen zu übertreffen.

Erfolgreich hergestellte Lang- und Kurzkanal p- und n-typ SB-MOSFETs mit und ohne Dotierstoffsegregation werden durch DC-Messungen charakterisiert. Transistoren

mit 80 nm Kanallänge zeigen dabei hohe An-Ströme von 427 μA/μm für p-typ und 1150 μA/μm für n-typ MOSFETs, welche vergleichbar zu anderen hochmodernen SB-MOSFETs sind.
Erstmalig werden durch Streuparameter-Messungen die extrinsischen und intrinsischen Eigenschaften von n- und p-typ SB-MOSFETs mit NiSi extrahiert. Die Hochfrequenzeigenschaften der Bauelemente zeigen ein perfekt lineares Skalierungsverhalten und hohe Grenzfrequenzen von 140 GHz für n-typ und 63 GHz für p-typ SB-MOSFETs mit einer Kanallänge von 80 nm. Die Optimierung des reproduzierbaren Herstellungsprozesses verbesserte die Source/Drain Widerstände um 30% auf 508 $\Omega\mu$m für Bauelemente, die auf 20 nm dünnem SOI hergestellt wurden. Obwohl die DC Leistungsfähigkeit der SB-MOSFETs durch eine hohe Schottky-Barriere stark veschlechtert wird, hat diese nur einen geringen Einfluß auf die Grenzfrequenz. Dies kann durch das gleiche Verhalten der Transkonduktanz und der Gate-Kapazität bei veränderten Implantationsdosen und damit Schottky-Barrier-Höhen erklärt werden. Ein Vergleich der Grenzfrequenzen mit hochmodernen MOSFETs verdeutlicht die ausgezeichnete Leistungsfähigkeit der hergestellten Bauelemente und deutet eine eindrucksvolle Verbesserung dieser für eine weitere Miniaturisierung an. Parameter, welche die Hochfrequenzeigenschaften limitieren und die Ursache für eine Variabilität der Leistungsfähigkeit der SB-MOSFETs werden eingehend diskutiert.
Zusammenfassend zeigt diese Arbeit ein hohes Potential der NiSi S/D SB-MOSFETs mit Dotierstoffsegregation für eine Nutzung in der hochgradig skalierten Mikroelektronik auf.

Abstract

The continuous downscaling of the Si-based microelectronics, which is the fundament of today's information technology, requires novel concepts for the source/drain (S/D) architecture of metal-oxide-semiconductor field-effect transistors (MOSFETs). The improvement of the carrier injection is of prime importance because of the increasing impact of parasitic resistances which strongly limit the performance of ultimately scaled transistors. Moreover, steeper junctions at the contact/channel interfaces become more and more crucial for nanoscale devices. In this context, Schottky-barrier (SB) MOSFETs with metallic S/D are promising performance boosters since they offer low extrinsic resistances and atomically abrupt junctions formed at the metal/silicon interface. However, a drawback of these devices is their performance which is inferior to conventional MOSFETs due to the relatively high Schottky barrier. Recently, dopant segregation has attracted much interest since the highly doped layer formed at the silicide/silicon interface during silicidation strongly improves the tunneling probability of carriers through Schottky contacts.

The present thesis studies the integration of NiSi with dopant segregation in SB-MOSFETs on thin-body silicon-on-insulator experimentally. The objective of the detailed direct-current (DC) and radio-frequency (RF) characterization is to gain a better insight into the physics of these devices.

The modeling of NiSi/p-Si Schottky contacts using a numerical model which combines the thermionic emission theory with image-force induced barrier lowering and quantum-mechanical tunneling provides a solid understanding of the carrier injection of Schottky contacts. The characterization of Schottky diodes with silicidation induced dopant segregation using boron, arsenic and antimony reveals effective Schottky barrier heights in the 0.1 eV regime depending on the implantation dose. Below this value SB-MOSFETs are capable of outperforming conventional MOSFETs.

Successfully fabricated long- and short-channel p- and n-type SB-MOSFETs with and without dopant segregation are characterized performing direct-current (DC) measurements. Transistors with 80 nm channel length reveal on-currents as high as $427\,\mu\mathrm{A}/\mu\mathrm{m}$ for p-type and $1150\,\mu\mathrm{A}/\mu\mathrm{m}$ for n-type devices, respectively, which compete well with state-of-the-art SB-MOSFETs.

For the first time, the extrinsic and intrinsic device parameters of short-channel n- and p-type NiSi SB-MOSFETs are extracted using scattering parameter measurements. The radio-frequency (RF) investigation of the devices reveals a perfectly linear scaling and high cut-off frequencies of 140 GHz for n-type and 63 GHz for p-type SB-MOSFETs with a gate length of 80 nm. The optimization of the reproducible fabrication process improves the S/D resistances by 30% and yields a value of 508 $\Omega\mu$m for devices fabricated on 20 nm thick silicon-on-insulator. Although, the DC performance of SB-MOSFETs is strongly deteriorated by high Schottky barriers, it has only a small impact on the cut-off frequency. This can be explained by the similar behavior of the transconductance and the total gate capacitance when the implantation dose and therefore the Schottky barrier height is changed. The benchmarking of the obtained cut-off frequencies with state-of-the-art MOSFETs demonstrates the superior RF performance of the fabricated devices and predicts an impressive performance increase for further downscaling. RF performance limiting parameters are identified and the origin of the RF variability of SB-MOSFETs is discussed.

In summary, the results of this work demonstrate a high potential of NiSi S/D SB-MOSFETs with dopant segregation for a use in ultimately scaled microelectronics.

Contents

Chapter 1

Introduction

The fundament of today's information technology is the Si-based microelectronics whose tremendous miniaturization has allowed the fabrication of increasingly powerful microprocessors and memory chips. The continuous downscaling of the integrated circuits in microelectronics was predicted by Gordon E. Moore in 1965. His empirical observation, the so-called Moore's law, states that the number of transistors which can be placed at low-costs on an integrated circuit is doubled every two years [1]. During the past 40 years, the microelectronics industry has followed Moore's law and the transistor feature size was scaled from 10 μm to approximately 30 nm, guided by the International Technology Roadmap for Semiconductors (ITRS). The objective of the ITRS which is adapted every second year is to ensure cost-effective advancements in the performance of the integrated circuits and the products that employ such devices, thereby continuing the health and success of the semiconductor industry [2].
While the performance increase has mainly relied on the scaling of the device dimensions, physical and technological limits are reached as the complementary metal-oxide-semiconductor (CMOS) technology is entering the decananometer regime. One of the most important challenges for ultimately scaled metal-oxide-semiconductor field-effect transistors (MOSFETs) is the improvement of the carrier injection because of the increasing impact of the parasitic resistances on the transistor performance [3]. Optimized S/D architectures are of prime importance for enhancing the on-current of MOSFETs which is required, for instance, for high radio-frequency (RF) performance. Schottky barrier (SB) MOSFETs with metallic S/D electrodes are regarded as an attractive alternative to conventional MOSFETs with highly doped S/D regions since they offer superior scaling abilities due to low extrinsic resistances and atomically abrupt junctions formed at the metal/silicon interface [4]. These benefits are complemented by low formation temperatures of the typically used silicides and a CMOS

compatible process flow. Especially, for ultimately scaled, fully depleted ultra-thin body (UTB) silicon-on-insulator (SOI) MOSFETs, metallic S/D junctions are promising performance boosters, as the electrical properties of these devices are strongly limited by parasitic resistances.
The concept of SB-MOSFETs, was first proposed by Nishi in 1966 and patented in 1970 [5]. In 1968 Lepselter and Sze published the first paper on SB-MOSFETs using PtSi S/D [6]. However, SB-MOSFETs exhibit an intrinsic performance inferior to conventional devices due to the Schottky barrier formed at the metal/channel interfaces. As a result, they suffer from low on-currents, a poor subthreshold swing and ambipolar switching. Recently, simulations have demonstrated that SB-MOSFETs with Schottky barrier heights (SBH) lower than 0.1 eV are capable of outperforming conventional MOSFETs [7, 8]. Therefore, over the last few years intensive research on SB-MOSFETs has been devoted to improve the carrier injection. As a result, three main concepts have been investigated.

- The use of rare-earth silicides like ErSi [9, 10] or YbSi [11] for n-MOSFETs and PtSi [11–13] for p-MOSFETs with the lowest known Schottky barrier heights for electrons (0.27-0.36 eV) and holes (0.15-0.27 eV), respectively, has shown impressive results.

- Fermi level depinning with an insulator placed between the metallic electrode and the semiconductor is an alternative to reduce the Schottky barrier height [14–16].

- Another very promising approach is the combination of silicides like PtSi or the midgap material NiSi with dopant segregation. Different techniques with implantation to silicide (ITS) followed by a drive-in anneal [17, 18], implantation to metal (ITM) [17] and the silicidation induced dopant segregation [4, 19] have been reported. In all cases dopants pile-up at the silicide/silicon interface during dopant segregation and form a thin highly doped layer which causes a strong band bending. As a consequence, the tunneling probability of carriers through the effectively lowered Schottky barrier increases significantly. Recent theoretical investigations consider the Schottky barrier height modulation as a result of dopant induced dipoles formed at the NiSi/Si interface [20–22].

Key benefits of dopant segregation using NiSi are easy formation, low costs, CMOS compatibility and much lower Schottky barrier heigths if compared to the other proposed methods. Therefore, the present thesis studies the use of NiSi in combination

with dopant segregation as silicide for SB-MOSFETs on thin-body SOI experimentally. A detailed direct-current (DC) and radio-frequency (RF) characterization offers physical insights into these devices.

- **Chapter 2** Fundamentals and device concepts of MOSFETs are introduced, including short-channel effects which deteriorate the performance of ultimately scaled devices. Moreover, this chapter explains the key device parameters which are used for device characterization and benchmarking.

- **Chapter 3** Since NiSi is used for the fabrication of SB-MOSFETs, the formation of nickel-silicides is discussed briefly and fundamentals of silicidation induced dopant segregation are presented.

- **Chapter 4** The physical modeling of NiSi/p-Si Schottky contacts using an appropriate numerical transport model provides a solid understanding of the carrier injection of Schottky contacts. A quantitative analysis of Schottky diodes with dopant segregation is performed by temperature-dependent I-V measurements and the extraction of the effective Schottky barrier heights. This chapter provides the fundamentals which are necessary to understand SB-MOSFET operation with and without dopant segregation.

- **Chapter 5** The development of a mask layout and a reproducible process technology facilitates the fabrication of long-channel as well as short-channel SB-MOSFETs. The ground-signal-ground (GSG) layout of the two-finger SB-MOSFETs in combination with dedicated test structures allows for RF characterizations.

- **Chapter 6** Successfully fabricated p- and n-type SB-MOSFETs with and without dopant segregation are characterized using direct-current (DC) measurements. Peculiarities of these SB-MOSFETs are discussed and key device parameters are extracted from the I-V charactersitics. Moreover, the 80 nm-short channel devices are compared with state-of-the-art SB-MOSFETs.

- **Chapter 7** After introducing the fundamentals of the scattering (S) parameter theory and the small-signal equivalent circuit of MOSFETs, this chapter provides for the first time a detailed RF analysis of dopant-segregated p- and n-type NiSi SB-MOSFETs. The S-parameter measurements facilitate the extraction of the extrinsic and intrinsic device parameters as a function of the device dimensions and implantation dose, i. e., the Schottky barrier height. The 80 nm-short channel devices are compared with state-of-the-art MOSFETs and a trend of the

performance increase of the fabricated SB-MOSFETs is given. Finally, the most important parameters which limit the RF performance are identified.

- **Chapter 8** This chapter discusses the variability of the RF performance of SB-MOSFETs and elaborates their origin.

Chapter 2

Basic Principles

This chapter gives an introduction to the most important fundamentals and device concepts of metal-oxide-semiconductor field-effect transistors (MOSFETs). After considering the MOS capacitor which provides the knowledge for an understanding of MOS-related devices, the basic principles of MOSFETs are introduced. Next to the examination of long-channel devices, the specific characteristics of short-channel MOSFETs are presented and discussed. Finally, the advantages of silicon-on-insulator substrates are presented and the crucial impact of parasitic resistances and capacitances is discussed.

2.1 The MOS Capacitor

Fig. 2.1 shows a cross-section of an ideal MOS capacitor with its energy-band diagram in the case of a p-type semiconductor at equilibrium ($V = 0$). Note, that the difference between the metal work function Φ_m and the semiconductor work function is zero:

$$V_{ms} = \Phi_m - \left(\chi_{Si} + \frac{E_G}{2q} + \Phi_{bp} \right) = 0 \tag{2.1}$$

χ_{Si} is the electron affinity of the semiconductor, E_G the bandgap and Φ_{bp} the difference between the intrinsic Fermi level E_i and the valence band edge E_V. Under this condition the conduction and valence bands are flat (flat-band condition) at equilibrium according to the requirement of a common Fermi level throughout the structure.

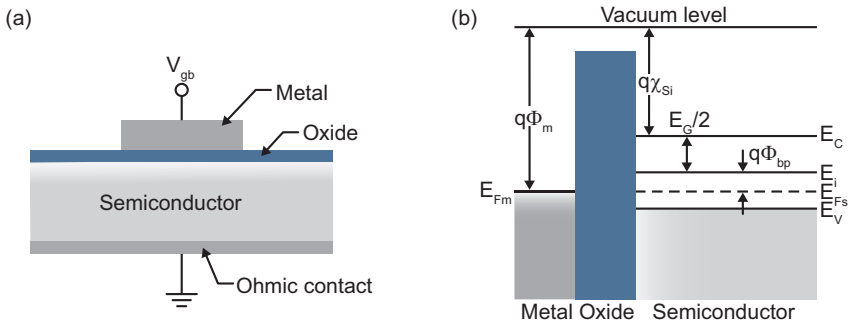

Figure 2.1: (a) Illustration of the MOS capacitor. (b) Energy band diagram of an ideal MOS capacitor built on a p-type semiconductor at equilibrium ($V = 0$). q: elementary charge, Φ_m: metal workfunction, χ_{Si}: electron affinity for semiconductor, E_G: bandgap, E_{Fm}, E_{Fs}: Fermi level of the metal and the semiconductor, E_C: bottom edge of the conduction band, E_V: top edge of the valence band, E_i: intrinsic Fermi level.

When a MOS capacitor is biased with an external voltage a surface potential Φ_s arises at the semiconductor-insulator interface and changes its charge distribution. In the depletion approximation the voltage dependence of the surface potential can be written as [23]:

$$V_{gb} = V_{fb} + \Phi_s - \frac{Q_S}{C_{ox}} = V_{fb} + \Phi_s + \frac{\sqrt{2\varepsilon_{Si} q N \Phi_s}}{C_{ox}} \tag{2.2}$$

where V_{fb} is flat-band voltage, C_{ox} the oxide capacitance, N the doping concentration of the semiconductor and ε_{Si} the permittivity of the semiconductor. Depending on the applied external voltage V_{gb} different cases of the surface potential Φ_s, illustrated in Fig. 2.2, can be distinguished [24]:

- $\Phi_s < 0$ (accumulation): When V_{gb} is smaller than the flat-band voltage V_{fb} holes accummulate at the oxide/semiconductor interface, which results in an upward band bending.

- $\Phi_s = 0$ (flat-band): The bands are flat and show no bending (Fig. 2.1(b)). The applied voltage V_{gb} compensates possible differences of the workfunctions of the metal and the semiconductor.

- $\Phi_{bp} > \Phi_s > 0$ (depletion): For $V_{gb} > V_{fb}$ holes are depleted from the interface leading to a lower hole concentraton than in the p-type bulk-Si which results in a downward band bending.

- $2\Phi_{bp} > \Phi_s > \Phi_{bp}$ (weak inversion): When V_{gb} becomes sufficiently positive to attract a significant number of free electrons to the silicon/oxide interface, the electron density will exceed the hole density at the interface.

- $\Phi_s > 2\Phi_{bp}$ (strong inversion): With further increase of V_{gb} the Fermi level E_{Fs} lies well above the intrinsic Fermi level E_i. The change of the surface potential Φ_s with the gate voltage is more and more reduced because the inversion charge screens the electric field generated by V_{gb}.

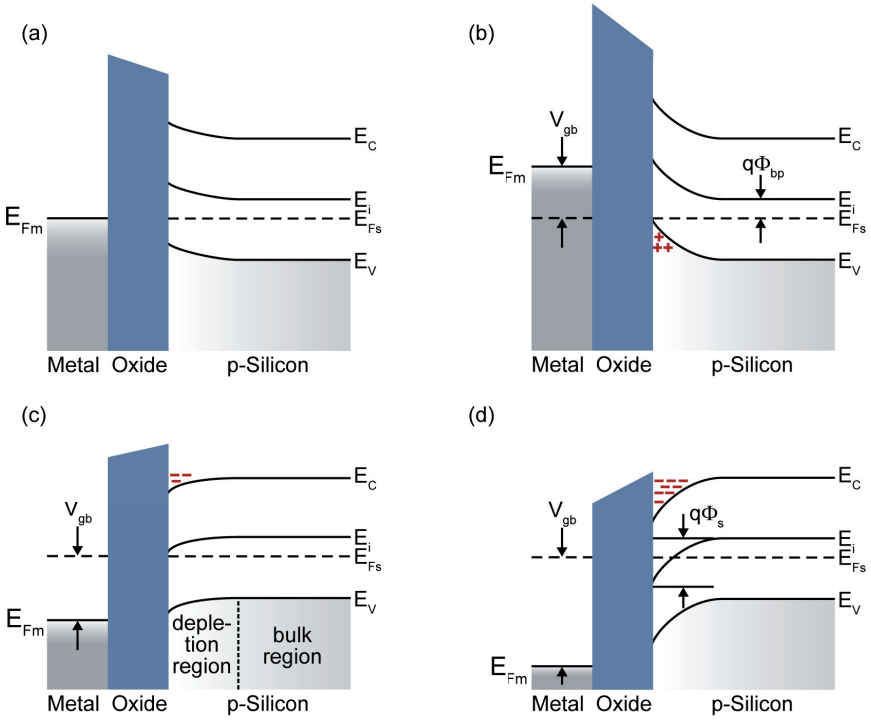

Figure 2.2: The MOS capacitor in (a) equilibrium, (b) accumulation, (c) onset of inversion and (d) strong inversion.

2.2 Fundamentals of MOSFETs

The MOSFET is a three terminal structure which consists of a MOS capacitor with highly conducting contacts to the left and to the right of the inversion layer. Fig. 2.3 illustrates an n-type MOSFET fabricated on a p-type silicon substrate. The two reverse

poled pn-junctions, "source" and "drain", are created by ion implantation with donors like As or P in a p-type substrate. The source is the contact with the lowest applied potential whereas drain is the one with the highest applied potential [25]. Separated by a thin insulating gate oxide with the thickness t_{ox} the gate electrode "gate" is located between source and drain (S/D). The current flow takes place in the inversion layer of

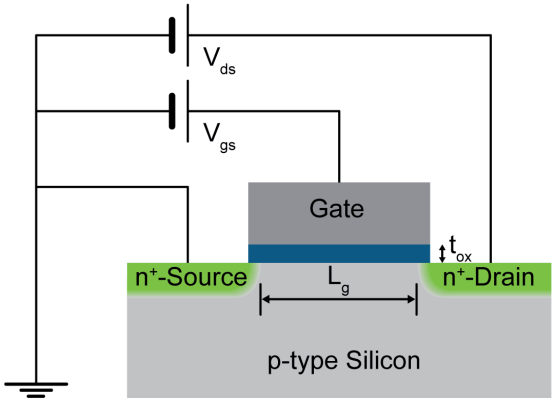

Figure 2.3: Sketch of the MOSFET with the channel length L_g, the gate oxide thickness t_{ox} and a typical circuitry showing the applied external voltages.

the p-type substrate between the source and drain contacts, whose distance determines the channel length L_g. Fig. 2.3 presents also the usually used common-source circuitry with the applied external voltages V_{gs}, the gate-source voltage, and V_{ds}, the drain-source voltage.

Please note that the following considerations will be discussed exclusively for the case of an n-type MOSFET, but can easily be transferred to p-type devices by appropriate change of the signs and parameters. At low gate-source voltages, the MOSFET is in its off-state and very little current flows in response to a drain-source voltage because of the potential barrier in the channel (black solid line in Fig. 2.4). When a positive V_{gs} is applied to the gate the conduction and valence band edges in the channel are lowered while the Fermi level E_F is fixed by the source and drain voltages which are assumed to be in equilibrium ($V_{ds} = 0$). This results in a higher conductivity of the channel and turns the transistor on. The threshold voltage V_T which is needed to turn the transistor on is determined by the energy difference between the equilibrium Fermi level E_F and the conduction band edge in the channel.

Applying a positive drain-source voltage lowers the conduction and valence band edges in the drain with respect to the source (orange solid line in Fig. 2.4). Hence, the Fermi levels of source E_{Fs} and drain E_{Fd} are separated by qV_{ds}:

$$E_{Fs} - E_{Fd} = qV_{ds} \tag{2.3}$$

Consequently, the channel is in a non-equilibrium state. For a simple system with the energy E, an expression for the steady-state current can be obtained [26]:

$$I_d \propto \frac{2q}{h} \int_{-\infty}^{\infty} T(E)[f_s(E) - f_d(E)]dE \tag{2.4}$$

where h is the Planck constant, $T(E)$ the transmission probability and f_s/f_d the Fermi-functions of source/drain. This simple equation illustrates basic facts of the transistor operation. If $f_s(E) = f_d(E)$ no current will flow. For energies significantly below E_{Fs} and E_{Fd}, $f_s(E) = f_d(E) = 1$ and consequently no current flows, as well as for energies well above E_{Fs} and E_{Fd} where $f_s(E) = f_d(E) = 0$. This means, that a drain current I_d will only flow for energies which lie within a few k_BT of the potentials E_{Fs} and E_{Fd}.

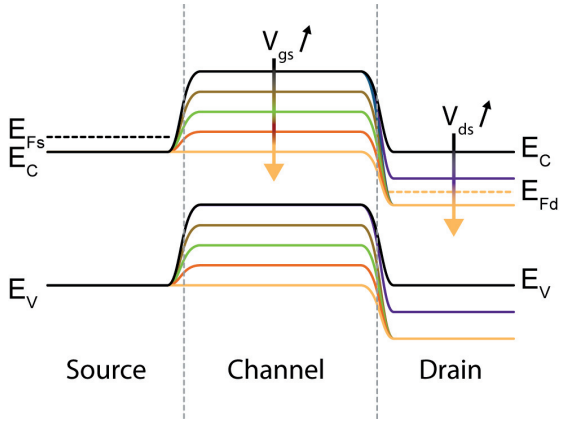

Figure 2.4: Band diagram of an n-channel MOSFET. The black line represents the off-state of the transistor ($V_{gs} = 0$, $V_{ds} = 0$), passing into the on-state with $V_{gs} > 0$, $V_{ds} > 0$ (orange line).

2.3 Long-Channel MOSFET

In case of long-channel MOSFETs the channel length L_g is much longer than the depletion zones of the pn-junctions at S/D. Therefore, these depletion zones can be neglected. In the gradual-channel approximation, which is the base for the following description of the basic MOSFET characteristics, the potential distribution can be

regarded as one-dimensional [27]. One key assumption of this approximation is that the variation of the transverse electric field E_z perpendicular to the channel is much larger than the corresponding variation of the longitudinal field E_x along the channel. Therefore, the behavior of the MOSFET is mainly determined by the potential along the z-direction. A second assumption which allows the derivation of analytical solutions for the drain current is the charge sheet model in which the inversion layer is treated as a charge sheet with zero thickness [28]. This gives the following equation for the drain current:

$$I_d = \frac{W_g}{L_g}\mu_{eff}C_{ox}\left\{\left(V_{gs} - V_{fb} - 2\Phi_{bp} - \frac{V_{ds}}{2}\right)V_{ds} - \frac{2}{3}\frac{\sqrt{2\varepsilon_0\varepsilon_{Si}qN_A}}{C_{ox}}\left[(V_{ds} + 2\Phi_{bp})^{3/2} - (2\Phi_{bp})^{3/2}\right]\right\} \tag{2.5}$$

W_g is the gate width, μ_{eff} the carrier mobility, ε_0 the dielectric constant, ε_{Si} the permittivity of the semiconductor and N_A the acceptor impurity concentration. Equation 2.5 predicts for a given gate-source voltage V_{gs} three different regions, that are the linear, the nonlinear and the saturation region which are depicted in the output characteristics I_d-V_{ds} in Fig. 2.5(a).

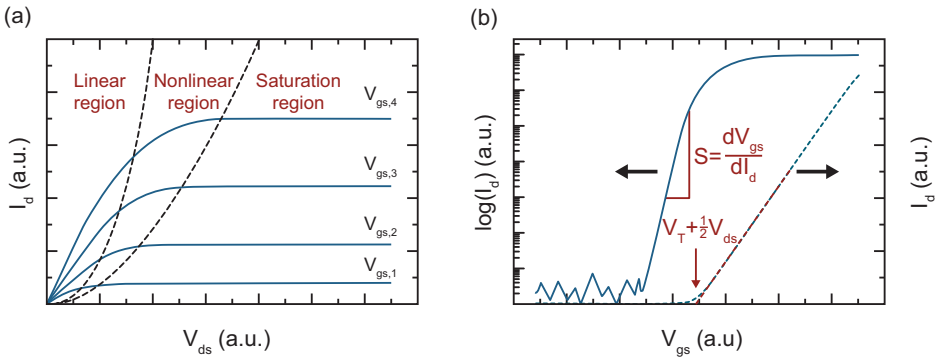

Figure 2.5: (a) Idealized output characteristics ($I_d - V_{ds}$) of a MOSFET. The dashed lines separate the linear, non-linear and saturation regions. (b) Transfer characteristic ($I_d - V_{gs}$) in logarithmic and linear scale show the inverse subthreshold slope S and the threshold voltage V_T.

For small V_{ds} Equation 2.5 reduces to

$$I_d = \frac{W_g}{L_g}\mu_{eff}C_{ox}\left(V_{gs} - V_T - \frac{V_{ds}}{2}\right)V_{ds} \tag{2.6}$$

with the threshold voltage V_T, given by

$$V_T = V_{fb} + 2\Phi_{bp} + \frac{\sqrt{2\varepsilon_{Si} q N_A (2\Phi_{bp})}}{C_{ox}} \tag{2.7}$$

Equation 2.6 indicates that, in the linear region, the MOSFET behaves like a resistor with a sheet resistivity $\rho_{sh} = 1/\left[\mu_{eff} C_{ox} (V_{gs} - V_T)\right]$ which can be modulated by the gate-source voltage V_{gs}. With increasing V_{ds} the drain current passes the non-linear region and saturates at I_{dsat} which can be obtained by setting $dI_d/dV_{ds} = 0$:

$$I_{dsat} = \frac{1}{2n} \frac{W_g}{L_g} \mu_{eff} C_{ox} (V_{gs} - V_T)^2 \tag{2.8}$$

n is the so-called body-factor, with $n = 1 + \frac{C_c}{C_{ox}}$, which depends on the oxide capacitance C_{ox} and on the capacitance of the depletion layer C_c. In the following, the occurance of drain current saturation is discussed in more detail using a simple model which is based on ballistic transport [26, 29, 30]. At the top of the potential barrier in the channel, electrons coming from the source have positive velocities and those coming from the drain have negative velocities. The positive velocity states $+k$ in the channel are filled up from the source with a Fermi level E_{Fs} while negative velocity states, $-k$ states, are filled up from the drain with a Fermi level E_{Fd}, which is illustrated in Fig. 2.6 . In the energy range between E_{Fs} and E_{Fd} the $+k$ states are nearly filled and carry current, which cannot be balanced by the $-k$ states since they are nearly empty. Therefore, the net current is proportional to $(E_{Fs} - E_{Fd})$. When E_{Fd} drops below the bottom of the conduction band edge E_C of the channel, the drain current cannot increase anymore and saturates at I_{dsat} which is proportional to $(E_{Fs} - E_C)$. This result is based on the assumption, that the only effect of the increasing V_{ds} is to lower E_{Fd}. However, it is possible, that the energy bands in the channel do not remain fixed relative to the source when V_{ds} is changed which occurs in short-channel MOSFETs (Chapter 2.5). In this case, the maximum potential barrier that determines the injection of carriers into the channel would would drop by some fraction of the drain potential $-qV_{ds}$ depending on the electrostatics. As a consequence, the band edge in the channel would be lowered resulting in an increase of I_{dsat} [26].
Fig.2.5(b) shows the transfer characteristics I_d-V_{gs} of a long-channel MOSFET. The logarithmic and linear scale plots allow the extraction of several important DC-parameters, which are described in the next section.

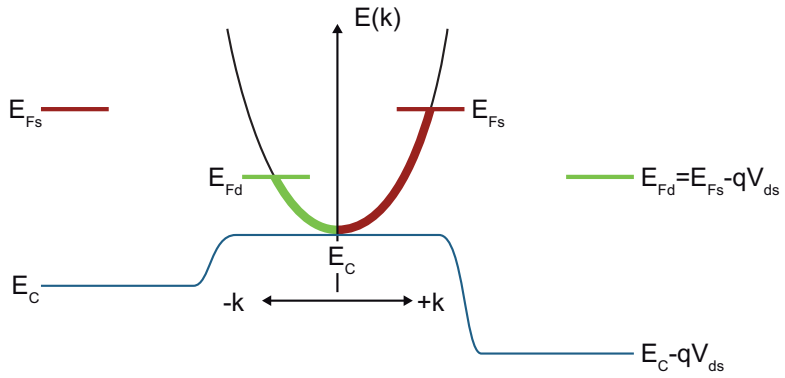

Figure 2.6: Illustration of how the k-states in the channel are filled by the Fermi levels of source and drain. The $+k$ states are occupied from the source up to E_{Fs} while the $-k$ states are occupied from the drain up to E_{Fd}, causing a net current flow.

2.4 Important DC-Parameters

Threshold Voltage V_T

The threshold voltage V_T (cf. Equation 2.7) represents the onset of significant drain current flow. It may be essentially understood as the gate-source voltage V_{gs} at which the transition between weak and strong inversion takes place in the channel. A simple way to extract V_T is to deduce it from the linear plot of the transfer characteristics at a small drain bias ($V_{ds} \ll V_{gs}$) by extrapolation of the linear part of the curve to zero drain current flow and subtraction of $V_{ds}/2$ (see Fig. 2.5(b)). Although, numerous methods exist for the extraction of the threshold voltage [31, 32], the constant current method is used in this work when extracting statistical information from a large number of devices because this widely used technique facilitates an automatic V_T extraction. A typical value for the arbitrary constant drain current is $W_m/L_m = 1 \cdot 10^{-7}$ A where W_m and L_m are the mask designed gate width and length, respectively [33]. The disadvantage of the constant current method is that V_T depends on the arbitrarily chosen value of the drain current. For the analysis of all other measurements the second derivative method [34] is used which avoids the dependence of V_T on the series resistance. The value of V_T is determined as the gate-source voltage at which the derivative of the transconductance g_m, i. e., $dg_m/dV_{gs} = d^2I_d/dV_{gs}^2$, is maximum. The weakness of this method is that it is highly sensitive to measurement errors and noise.

Inverse Subthreshold Slope S

The inverse subthreshold slope S quantifies which gate-source voltage range is needed to switch a MOSFET from the off-state to the on-state. It is defined as the gate-source voltage needed to increase the drain current by one order of magnitude [24]:

$$S = \ln(10)\,\frac{k_B T}{q}\left(1 + \frac{C_C}{C_{ox}}\right) \qquad (\mathrm{mV/dec}) \tag{2.9}$$

C_C is the capacitance of the semiconductor space-charge region where the electrical charges are composed of the inversion layer charge and ionized acceptor atoms forming the depletion layer charge. The inverse subthreshold slope can be determined by linear fitting of the logarithmic transfer characteristics, see Fig. 2.5(b). The theoretical minimum of S is 60 mV/dec at room temperature for devices with thermal injection of carriers. Recently, band-to-band tunneling transistors have attracted much interest since they potentially offer the ability of having inverse subthreshold slopes less than 60 mV/dec due to field-effect controlled band-to-band tunneling [35–39].

Transconductance G_m

The transconductance G_m of a MOSFET is a measure of the gate control over drive current modulation. It is given by the first derivative of I_d with respect to V_{gs}:

$$G_m = \left.\frac{dI_d}{dV_{gs}}\right|_{V_{ds}} \qquad (\mathrm{S}) \tag{2.10}$$

In general, G_m increases in inverse proportion to the gate length L_g. However, when the gate length falls to the deep submicrometer level the increase drops off, because the S/D resistance and velocity saturation of carriers limit G_m [40].

Gate Induced Drain Leakage

A large component of off-state leakage current is gate induced drain leakage (GIDL), caused by band-to-band tunneling in the drain region underneath the gate stack. It occurs when the gate-to-drain bias is sufficient that the energy-band bending close to the Si/gate-dielectric interface is large enough that valence-band electrons can tunnel into the conduction band. GIDL is an obstacle for gate-oxide thickness scaling because the voltage required to cause this band-to-band tunneling current decreases with the gate oxide thickness. Especially for low-power circuit applications the off-state leakage current plays an important role. Moreover, GIDL can pose a lower limit for

standby power in memory devices, but it becomes less significant for digital logic applications where the power-supply voltage is reduced to below 1.1 V, corresponding to the energy band gap of silicon [41]. GIDL appears in the transfer characteristics as a V_{ds}-dependent off-state current which is indicated in Fig 2.7(b). A similar off-current branch is observed for SB-MOSFETs due to an ambipolar switching behavior, which is discussed in Chapter 6.2.

Mobility μ_{eff}

The mobility μ_{eff} is defined as the proportionality constant between the drift velocity v_x and the electric field strength E_x at low electric fields:

$$v_x = \mu_{eff} \cdot E_x \tag{2.11}$$

Carrier scattering with acoustic phonons and ionized impurities significantly affects the mobility of nonpolar semiconductors such as Si and Ge. In principle, two methods for the mobility extraction of MOSFETs are used. On the one hand, it is possible to use the $I_d/\sqrt{g_m}$-method which is a very simple method that is often used for the mobility extraction of Pseudo-MOSFETs [42]. On the other hand, split capacitance-voltage (C-V) measurements facilitate the extraction of μ_{eff} versus the effective field E_z which is perpendicular to the transport direction [43, 44].

2.5 Short-Channel MOSFETs

When the channel length decreases the spatial extent of the depletion widths of S/D become more and more comparable to the channel length. In this case, short-channel effects (SCE) arise as a result of a two-dimensional potential distribution and high electric fields in the channel region. The one-dimensional gradual-channel approximation ($E_z >> E_x$) is no longer valid and the potential distribution in the channel depends on the transverse electric field E_z as well as on the longitudinal field E_x. In the following, scaling rules are presented which ensure long-channel behavior of MOSFETs when the gate length is scaled down. Since deviations from this behavior cannot be avoided completely, the most crucial SCE are introduced.

2.5.1 Scaling Rules

Although, many scaling rules have been proposed [45, 46], the most-ideal rule to avoid SCE is to scale down all device dimensions and voltages of a long-channel MOSFET

in a way that the electric fields in the transistor are sustained [47]. This constant-field scaling includes a shrinking of all device dimensions and potentials by a factor $1/\kappa$ and an increase of the doping concentration by a factor κ, leading to a reduction of the depletion width. However, further downscaling becomes more and more complicated since the junction built-in voltage and the surface potential for the onset of weak inversion do not scale. Therefore, the supply voltage cannot be scaled as it is required in highly integrated circuits in order to reduce the power consumption. Moreover, physical limitations have become a major problem. Gate leakage currents induced by tunneling through the ultra-thin gate oxides [48] as well as increased S/D resistances $R_{s/d}$ when the junction depths are decreased have been huge challenges in the last few years. With these limitations scaling rules have been proposed which allow the adjustment of various device parameters independently as long as the transistor behavior is preserved [49]. According to reference [49] the channel length L_g must be larger than L_{min} in order to achieve long-channel behavior

$$L_{min} = 0.41\text{Å} \left[t_j t_{ox} \left(W_s + W_d \right)^2 \right]^{1/3} \tag{2.12}$$

with the implantation depth t_j, the gate-oxide thickness t_{ox} and the S/D depletion widths W_s and W_d. In the case of planar SOI MOSFETs which are introduced in Chapter 2.6 devices are free of short-channel effects if the effective gate length is larger than five to ten times the natural length λ [46]:

$$\lambda = \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{Si} t_{ox}} \tag{2.13}$$

where λ can be derived from Poisson's equation. The natural length of a device basically represents the length of the region of the channel that is controlled by the drain [50].

2.5.2 Short-Channel Effects

Though, the presented scaling rules should keep the long-channel behavior when devices are scaled down, SCE cannot be totally prevented. They are a result of a loss of the gate control as well as an increasing influence of the drain potential. In contrast to the transfer and output characteristics of long-channel MOSFETs, discussed in Chapter 2.3, short-channel devices show major differences in the electrical behavior. For example, the drain current I_d does not saturate at high V_{ds} (Fig. 2.7(a)). The threshold voltage shifts to lower values with increasing drain bias V_{ds} (Fig. 2.7(b)) and also with decreasing channel length L_g.

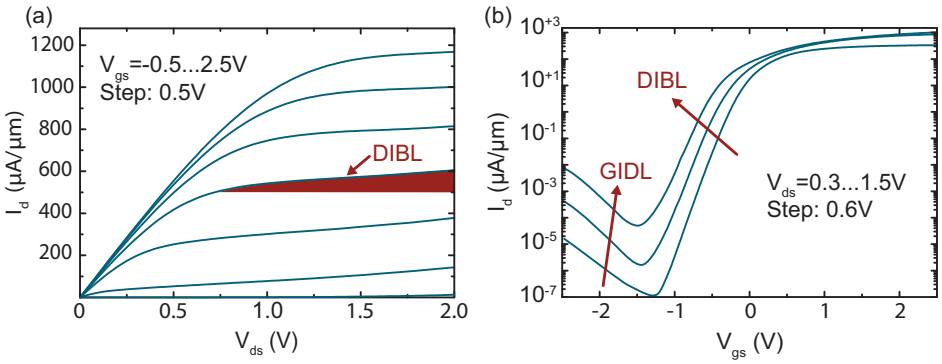

Figure 2.7: (a) Output characteristics and (b) transfer characteristics of a short-channel MOSFET showing DIBL and GIDL.

Drain Induced Barrier Lowering

Drain induced barrier lowering (DIBL) occurs, when the drain fields penetrate deeply into the channel which lowers the potential barrier near the source. This happens when the depletion zones of source and drain are a substantial fraction of the channel length. Fig. 2.8 shows the potential diagrams of a long- and a short-channel MOSFET for two different V_{ds} values. Whereas, the drain bias has no impact on the potential barrier in the channel in case of the long-channel MOSFET, the potential barrier varies with V_{ds} for the short-channel device. As a result, the subthreshold current and the threshold voltage V_T become bias dependent. This effect prevents the saturation of the drain current, which is clearly visible in Fig. 2.7(a) and results in a V_T-shift with increasing V_{ds}, Fig. 2.7(b). A measure for DIBL is the shift of the threshold voltage ΔV_T per incremental change of the drain bias ΔV_{ds}:

$$\text{DIBL} = \left| \frac{\Delta V_T}{\Delta V_{ds}} \right| \qquad \text{(mV/V)} \tag{2.14}$$

Punch-through

When the the sum of the depletion widths approaches the channel length ($L_g \leq 2\,\lambda$), a large V_{ds}-dependent leakage current occurs between source and drain. This condition is called punch-through.

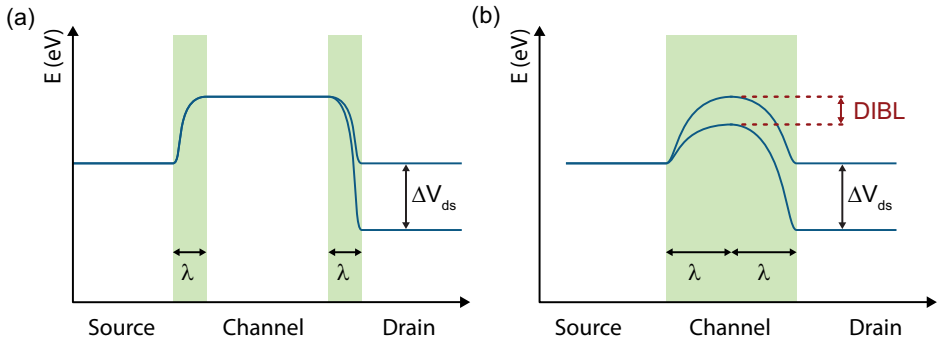

Figure 2.8: Potential diagram of a long-channel MOSFET with (a) $L_g > 5\lambda$ and (b) a short-channel MOSFET with $L_g \approx 2\lambda$ for two different V_{ds} values, illustrating DIBL for the short-channel device.

Threshold-Voltage Roll-off

Another DIBL-induced effect is the threshold voltage roll-off (V_T-roll-off) which also occurs when the depletion zones of source and drain become comparable to the channel length. The potential barrier in the channel is decreased with smaller gate length which results in a decrease of the threshold voltage compared to V_T of long-channel MOSFETs. This is a major technological challenge because tolerances of the gate length produced during the fabrication process lead to significant variability of V_T [51]. Next to the increase of the dopant level in the channel, a reduction of the gate oxide thickness and the use of ultra-shallow junctions to prevent SCE, the use of ultra-thin body silicon-on-insulator (UTB-SOI) substrates seems to be a promising way [42].

2.6 SOI Substrates

Silicon-on-insulator (SOI) substrates have attracted much attention during the last few years because of some inherent advantages of SOI devices over bulk CMOS. A thin crystalline silicon layer with the thickness t_{Si} on top of a thick SiO_2, the so-called buried oxide (BOX), allows the direct dielectric isolation of adjacent devices on a wafer. Depending on the silicon thickness t_{Si}, short-channel effects are strongly reduced. Moreover, the S/D junction capacitance is almost completely eliminated in SOI MOSFETs and the capacitance through the buried oxide layer to the substrate is very small [42]. Other advantages are the absence of the body effect and soft-error immunity due to a reduced volume which is susceptible to ionizing radiation

[23]. The electrical performance of SOI MOSFETs strongly depends on the silicon thickness t_{Si}. Therefore, SOI MOSFETs are often distinguished between partially depleted, when t_{Si} is thicker than the maximum gate depletion width and the device exhibits a floating body effect, and fully depleted, when t_{Si} is thin enough that the Si layer is fully depleted at the threshold condition. For $t_{Si} > 300\,\text{nm}$ the devices behave like bulk MOSFETs. Fully depleted ultra-thin body SOI (UTB SOI) MOSFETs with $t_{Si} \leq 20\,\text{nm}$ are regarded as the most promising candidates for a reduction of short-channel effects [42]. This can be understood by considering the distribution of depletion charges in a partially and a fully depleted short-channel SOI MOSFET with a simple geometrical construction [52], shown in Fig. 2.9. The upper base of the trapezoid is given by the gate length whereas the lower base is reduced due to the influence of source and drain. When the channel length is decreased, the lower base reduces until it passes away which happens earlier in case of the partially depleted or bulk device. In this case, most of the depletion charge Q_D is not controlled by the gate anymore, but by source and drain. Hence, partially depleted devices, as well as bulk MOSFETs, suffers more from SCE than fully depleted SOI MOSFETs.

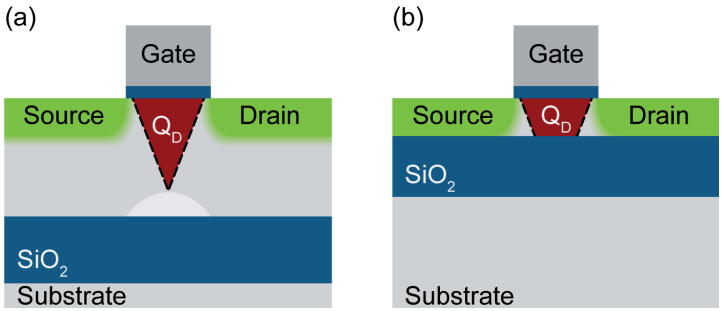

Figure 2.9: Distribution of depletion charges in partially (a) and fully (b) depleted short-channel SOI MOSFETs. Q_D is the depletion charge controlled by the gate.

Moreover, quantum mechanical effects which occur due to the z-confinement of the electron wave-function reduce SCE since the potential barrier in the channel is increased. The quantization gives rise to subbands such that the energy levels are no longer described by a parabolic relation like in a bulk solid with

$$E(\vec{k}) \approx E_C + \frac{\hbar^2 \left(k_x^2 + k_y^2 + k_z^2\right)}{2m_c} \tag{2.15}$$

but by a quasi-continuum of two-dimensional subbands (labeled with the index p) in

the channel that split up into energetically separated levels

$$E_p(k_x, k_y) \approx E_C + p^2\epsilon_z + \frac{\hbar^2\left(k_x^2 + k_y^2\right)}{2m_c}$$
$$\epsilon_z = \frac{\hbar^2\pi^2}{2m_c t_{Si}^2} \tag{2.16}$$

The increase of the potential barrier in the channel is especially important for short-channel MOSFETs with undoped channels to reduce short-channel effects and avoid punch-through. Drawbacks of the quantization are a reduction of the density of states in the channel and therefore a degradation of the MOSFET performance.

2.7 Parasitic Resistances and Capacitances

With downscaling of CMOS technology the S/D and contact sizes have to be scaled aggressively besides the gate length reduction, in order to increase the device density. This leads to small contact sizes which result in higher S/D resistances and contact-to-gate capacitances. In case of long-channel devices the parasitics do not play an important role because they are much smaller than the channel resistance and capacitance. However, in deeply scaled CMOS devices parasitics strongly limit the electrical performance. Since the channel resistance and capacitance decrease with the gate length, the parasitic resistances and capacitances are becoming comparable and can become even larger than the intrinsic device parameters [3]. Fig. 2.10 shows the parasitic and intrinsic resistances and capacitances versus the technology node and highlights the goal of the ITRS roadmap for the S/D resistance.
Especially, in fully depleted UTB SOI devices there are increasing concerns about the impact of the parasitic series resistances as no manufacturable solutions are known to achieve a S/D resistance of 200 Ωcm as it is recommended by the ITRS Roadmap [2]. Therefore, S/D engineering takes on an increasing importance in the development of leading edge CMOS generations in order to preserve current drive capability. The replacement of the conventionally implanted S/D regions by metals, typically silicides, which is regarded as a performance booster due to a reduction of the S/D resistance will be discussed in more detail in the following chapters. Since the fabrication and characterization of NiSi S/D SB-MOSFETs with low barrier heights is the main topic of this thesis the most important properties of nickel silcides are described in the next chapter.

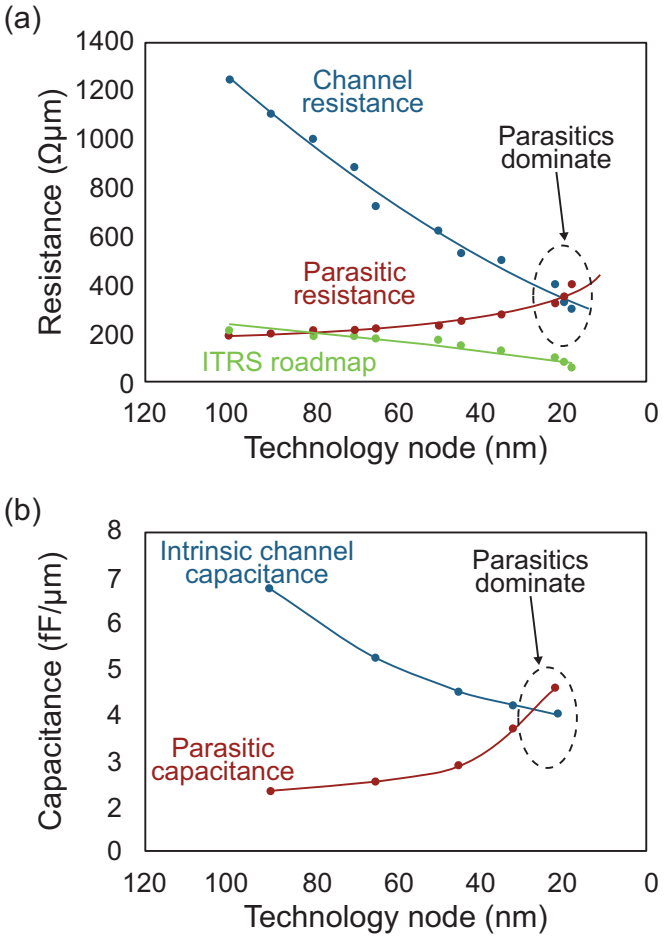

Figure 2.10: (a) Total planar CMOS parasitic and channel resistance versus technology node. (b) Total planar CMOS parasitic and intrinsic channel capacitance versus technology node. Note, that the parasitics are on course to become even larger than the intrinsic device parameters (after [3]).

Chapter 3

Nickel Silicide

This chapter briefly introduces nickel silicides and the advantages over other silicides like $TiSi_2$ and $CoSi_2$. The formation of NiSi is presented and fabricated NiSi layers on bulk Si and on SOI are investigated. The discussion of silicidation induced dopant segregation completes this part.

3.1 Introduction

The use of metal silicides in Si technology is related to basic requirements like low specific resistivity, low contact resistivity to p-type and n-type Si, high thermal stability and an excellent process compatibility with standard CMOS processing [53]. Nowadays, silicides are widely used as ohmic contacts, Schottky contacts and interconnects. Moreover, as the parasitic series resistances increase with device dimension scaling, as presented in Chapter 2.7, salicide (self-aligned silicide) processes have become an indispensable technique for high-performance CMOS fabrication. The reduction of the resistances is a major challenge, especially, for high-speed operation of digital circuits, but also for high-frequency and low-noise operation of RF circuits.
Although, various silicides like $TiSi_2$ and $CoSi_2$ have been investigated as materials for salicide processes, the midgap silicide NiSi offers major advantages for the sub-100 nm node, e.g. low silicidation temperature, low silicon consumption, no bridging failure property, smaller mechanical stress, no narrow-line effect on the sheet resistance and smaller contact resistance [54].
Strong drawbacks of rare earth silicides like ErSi and YbSi are the difficult formation and a Schottky barrier which is still too high. The disadvantage of PtSi are mainly the high costs.

3.2 Formation of NiSi

The silicide phases which may form during solid-state interactions between thin Ni films and a Si substrate are presented in Fig. 3.1. The Ni_xSi_y phase of interest is the NiSi phase with the lowest resistivity of 10.5 - 15 $\mu\Omega$cm (cf. Table 3.1). The crystal structure of this phase is orthorhombic, while $NiSi_2$ is cubic with a lattice constant close to the one of Si. The silicide formation with Ni as dominant moving species occurs during rapid thermal annealing after deposition of a thin Ni layer on Si. Depending on the annealing temperature different phases are formed; from metal-rich phases to mono-silicide and finally to Si rich phases:

$$\mathrm{Ni} \longrightarrow \alpha \longrightarrow \mathrm{Ni_2Si} \longrightarrow \mathrm{NiSi} \longrightarrow \mathrm{NiSi_2} \tag{3.1}$$

Formation temperatures T_f of Ni_2Si, NiSi and $NiSi_2$ are shown in Table 3.1.

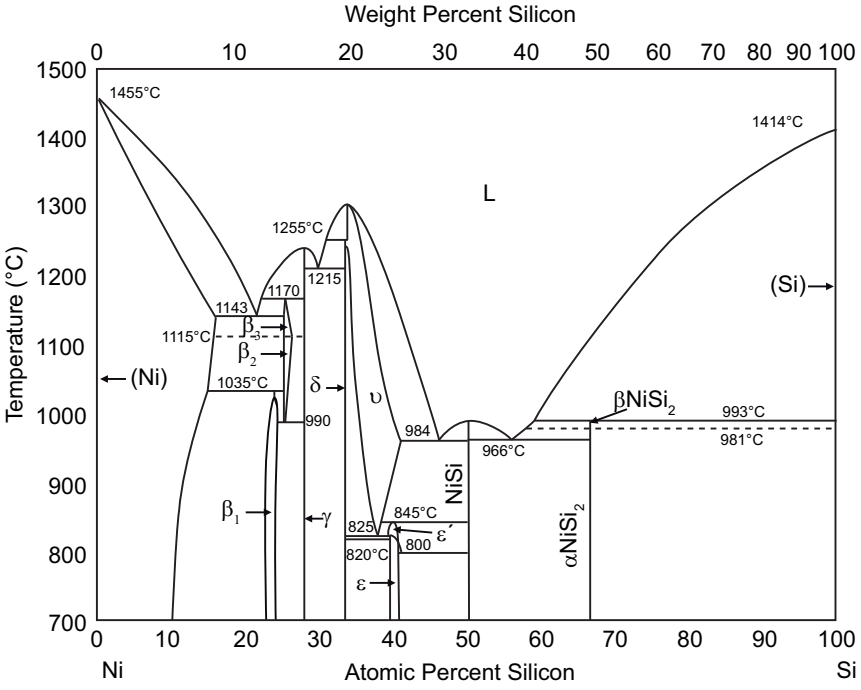

Figure 3.1: Binary phase diagram for NiSi after [53].

Phase	Crystal structure	Lattice constant (Å) a	b	c	T_f (°C)	ρ ($\mu\Omega$cm)
Ni_2Si	Orthorhombic	5.00	3.73	7.04	200-325	24
NiSi	Orthorhombic	5.18	3.34	5.62	350-600	10.5-15
$NiSi_2$	Cubic	5.40	—	—	750-800	34

Table 3.1: Properties of Ni_xSi_y phases [53]. T_f is the formation temperature; ρ the specific resistance.

For the characterization of the NiSi formation, 30 nm and 20 nm Ni is deposited by electron-beam evaporation on high-resistivity bulk Si(100) and 80 nm-thick SOI, respectively, directly after removing the native oxide. The samples are then annealed for 30 s at different temperatures ranging from 300°C to 800°C. Fig. 3.2 shows the sheet resistance of the formed NiSi layers measured using the Van-der-Pauw method as a function of the annealing temperature. From 400°C to 700° NiSi is the dominant phase with a constant sheet resistance R_{sh} of 2.0 Ω/□ for the thicker NiSi layer (69 nm) on bulk-Si and 2.9 Ω/□ for the thinner NiSi layer (46 nm) on SOI. The specific resistivity of the NiSi layer is approximately 13$\mu\Omega$cm which is in good agreement with literature data (cf. Table 3.1). R_{sh} increases for temperatures lower than 400°C where Ni_2Si is the dominant phase and also for temperatures higher than 700°C where $NiSi_2$ is formed.

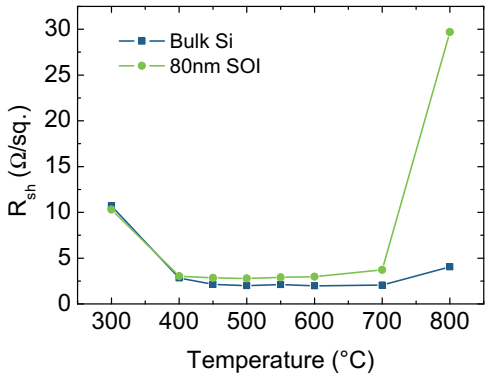

Figure 3.2: Sheet resistance R_{sh} of NiSi layers as a function of the annealing temperature.

Fig. 3.3 shows a cross-sectional transmission electon microscopy (TEM) image of a poly-crystalline NiSi layer on bulk-Si. Clearly visible is a roughness of the NiSi/Si interface whose effect on the electrical characteristics of SB-MOSFETs is discussed in

Chapter 8. The inferface roughness is quantitatively investigated with X-ray reflectivity (XRR) measurements for different annealing temperatures. Fig. 3.4(a) shows an XRR measurement of an 80 nm thick NiSi layer formed with a one-step annealing at 500°C for 30 s. The extracted root mean square (RMS) roughness of the NiSi/Si interface is 1.3 nm. While the roughness of the Ni-rich phases and the $NiSi_2$ phase is too large for the extraction of the RMS value, only the nickel mono-silicide phase is shown in Fig. 3.4(b). RMS values of approximately 1 nm are found for the NiSi/Si interface roughness whereas the NiSi surface roughness shows values of 4 nm.

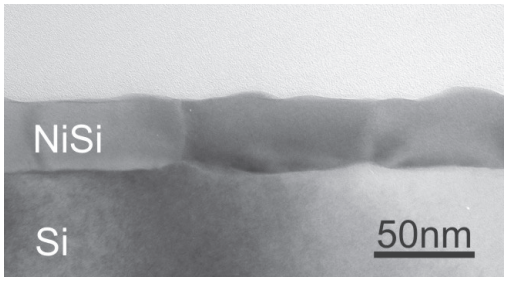

Figure 3.3: TEM image of a polycrystalline NiSi layer on bulk Si clearly showing the NiSi/Si interface roughness.

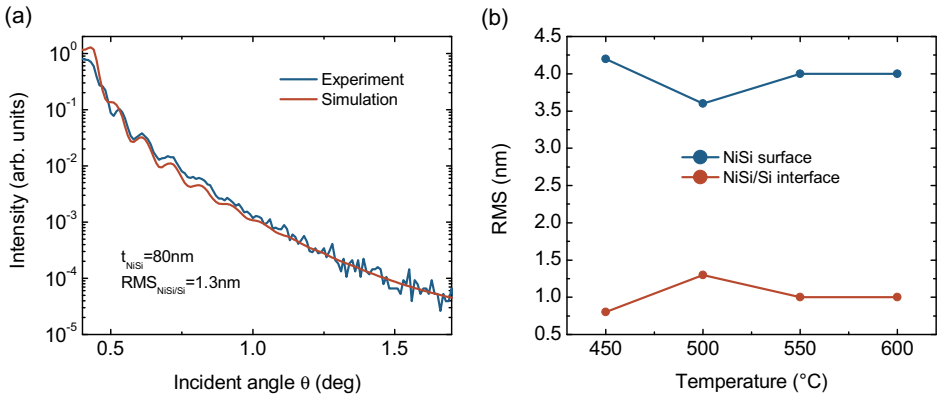

Figure 3.4: (a) XRR measurement of an 80 nm thick NiSi layer on bulk Si. (b) The NiSi/Si RMS roughness is around 1 nm for all temperatures where the nickel mono-silicide phase occurs.

3.3 Dopant Segregation

During the silicide formation on doped Si, the dopants are found to redistribute at the silicide/silicon interface. This concept of dopant segregation was introduced by R. Thornten in 1981 who used a thin p-type interfacial layer to rise the PtSi Schottky barrier on n-type Si [55]. During the silicidation induced dopant segregation, the dopants are expected to be snow-plowed by the growing silicide and become piled-up at the silicide/Si interface. Dopant segregation occurs if the solid solubility of the dopants in the silicide is low and point defects exist at the silicide/Si interface [56] and if the intrinsic diffusion of these dopants in Si is extremly low at the silicidation temperatures ($< 800°C$) [57]. A detailed description of the segregation mechanism can be found in Ref. [56].

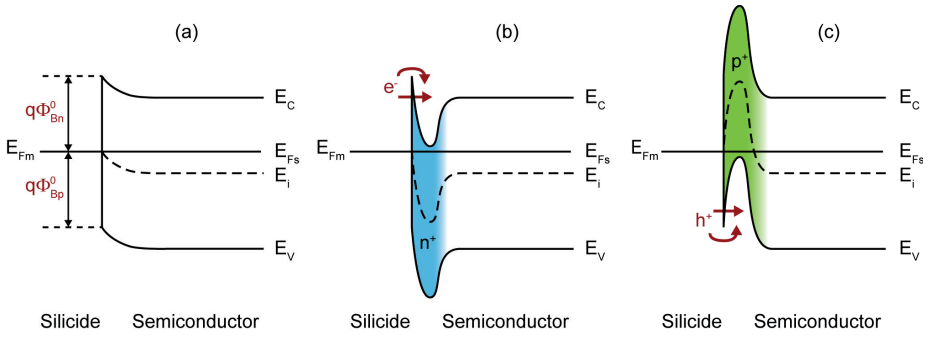

Figure 3.5: Schematic band diagrams of (a) a midgap silicide with equal Schottky barrier heights for electrons and holes, (b) band bending induced by segregated n-type dopants and (c) band bending induced by segregated p-type dopants (after [58]). The n^+ and p^+ segregation layers are indicated by a blue and green color gradient at the silicide/silicon interface.

The snow-plowed dopants in the silicon form a thin highly doped layer which causes a strong up- or downward band bending depending on the type of dopants. As a consequence, the tunneling probability of carriers through the effectively lowered Schottky barrier increases significantly. Although, dopant segregation is performed at relatively low temperatures, a fraction of dopants is located at substitutional sites in the silicon lattice and is therefore activated. Recent theoretical investigations using first principles calculations suggest that dopants at substitutional sites in the silicon lattice at the interface induce local dipoles which dominate the Schottky barrier height [20–22]. For instance, a B atom which is located at the substitutional site for a Si atom in the Si layer induces interface dipoles in opposite direction to the electric dipoles generated

by the energy difference between the Femi level of NiSi and the charge neutrality level of the semiconductor. As a result, the interface states, pinning the Fermi level, disappear and the Fermi level shifts closer to the valence band edge due to the induced dipoles around the B atom [20]. Consequently, the Schottky barrier height is reduced. Fig. 3.5 shows schematically the strong band bending at the NiSi/Si interface for a lightly doped n-type Si substrate with an n^+ and a p^+ segregation layer.

Chapter 4

Schottky-Diodes

A detailed analysis of the electrical characteristics of Schottky diodes is presented in this chapter to provide the background for an understanding of SB-MOSFETs, where the carrier injection is mediated by the source Schottky barrier. The physical background of current transport in metal/semiconductor contacts and neccessary modifications of the transport model for real applications are discussed. A systematic study of Schottky barrier height modulation is carried out using silicidation induced dopant segregation and the effective Schottky barrier heights are extracted as a function of the implantation dose.

4.1 Ideal Metal-Semiconductor Contacts

A Schottky barrier is formed at a metal-semiconductor interface which controls the current flow as well as the charge distribution of the contact. Fig. 4.1(a) shows ideal energy-band diagrams of a seperated metal and an n-doped semiconductor. When both materials are connected, which is illustrated in Fig. 4.1(b), charge will flow from the semiconductor to the metal until thermal equilibrum is reached, i.e the Fermi level of the metal E_{Fm} and of the semiconductor E_{Fs} line up. In this case, E_{Fs} is lowered relative to E_{Fm} by an amount equal to the difference of the two workfunctions, resulting in an upward band bending of the conduction and the valence bands.

Under these ideal conditions, the Schottky barrier height for electrons $q\Phi^0_{Bn}$ is simply the difference between the metal workfunction $q\Phi_m$ and the electron affinity of the semiconductor $q\chi$:

$$q\Phi^0_{Bn} = q\left(\Phi_m - \chi\right) \tag{4.1}$$

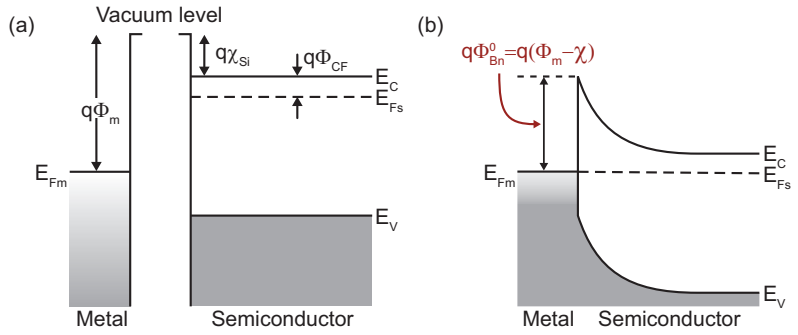

Figure 4.1: Energy-band diagrams of (a) a metal and an n-doped semiconductor and (b) of the Schottky contact at equilibrium.

A useful relationship is, that the sum of the barrier heights for electrons on n-type and holes on p-type substrates is expected to be equal to the bandgap E_g, i. e.,

$$E_g = q\left(\Phi^0_{Bn} - \Phi^0_{Bp}\right) \tag{4.2}$$

4.2 Current Transport in Schottky Contacts

In contrast to p-n junctions, the current transport in Schottky contacts is mainly due to majority carriers. The four transport mechanisms under forward bias, illustrated in Fig. 4.2, are:

- **Thermionic emission** of electrons over the potential barrier is the dominant transport mechanism for Schottky diodes on moderately doped semiconductors at room temperature.
- **Quantum-mechanical tunneling** of electrons through the Schottky barrier dominates the transport at low temperatures where thermionic emission dissappears and also for heaviliy doped semiconductors.
- **Recombination** of electrons and holes occurs in the space-charge or depetion region and in the neutral region, which represents the bulk-Si.
- **Diffusion of holes** which are injected from the metal and diffuse into the semiconductor.

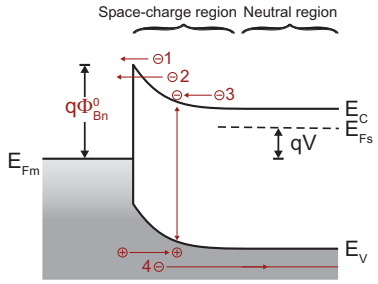

Figure 4.2: Current transport in Schottky contacts under forward bias qV. (1) Thermionic emission, (2) tunneling, (3) recombination and (4) diffusion of holes.

4.3 Thermionic Emission Theory

To derive the current-voltage characteristics of Schottky diodes on moderately doped semiconductors, thermionic emission is assumed to be the dominant current transport mechanism. The main assumption is that only carriers with energies larger than the Schottky barrier height $q\Phi^0_{Bn}$ are able to overcome the Schottky barrier and contribute to the current flow. Hence, the forward current density J_F is given by the concentration of electrons with energies sufficient to overcome the Schottky barrier and traversing from the semiconductor to the metal [24, 59]:

$$J_F = \int_{E_{Fm}+q\Phi^0_{Bn}}^{\infty} q v_x D(E) f(E) dE \tag{4.3}$$

where $E_{Fm} + q\Phi^0_{Bn}$ is the minimum energy required for thermionic emission into the metal. $D(E)$ and $f(E)$ are the density of states and the distribution function, respectively. After substitution of the integral from dE to an integral of the velocity dv we obtain:

$$J_F = A^* T^2 \exp\left(\frac{-q\Phi^0_{Bn}}{k_B T}\right) \exp\left(\frac{qV}{k_B T}\right) \tag{4.4}$$

with the effective Richardson constant for thermionic emission:

$$A^* = \frac{4\pi q m^* k_B^2}{h^3} \tag{4.5}$$

The Richardson constant has a value of $A^* = 120\,\mathrm{Acm^{-2}K^{-2}}$ for free electrons with $m^* = m_0$. Since the barrier height for electrons does not change under reverse bias, the current which is flowing from the metal into the semiconductor is unaffected by the applied voltage. Therefore, the forward current density J_F must be equal to the

reverse current density J_R at thermal equilibrium, i. e., $V = 0$:

$$J_R = -A^* T^2 \exp\left(\frac{-q\Phi_{Bn}^0}{k_B T}\right) \tag{4.6}$$

Finally, the total current for an area A is given by the sum of Eqs. 4.4 and 4.6.

$$I = I_F - I_R = I_0 \left[\exp\left(\frac{qV}{k_B T}\right) - 1\right] \tag{4.7}$$

with

$$I_0 = AA^* T^2 \exp\left(\frac{-q\Phi_{Bn}^0}{k_B T}\right) \tag{4.8}$$

4.4 Real Metal-Semiconductor Contacts

Current-Voltage Characteristics

The current-voltage characteristic of a Schottky diode, described by thermionic emission theory without considering parasitics, is presented in Fig. 4.3 by the blue solid line. Under reverse bias, the current flow is limited by the constant saturation current I_0 whereas an exponential current increase is observed if the diode is biased in forward direction.

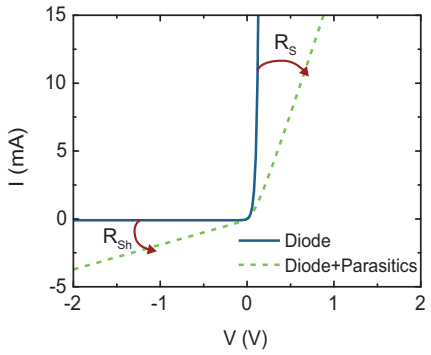

Figure 4.3: Current-voltage characteristics of a Schottky diode calculated with pure thermionic emission theory (blue solid line) and in combination with parasitic series resistance R_S and shunt resistance R_{Sh} (green dotted line).

However, real Schottky diodes show strong deviations from this ideal I-V-characteristic which is shown by the green dotted line in Fig. 4.3. On the one hand, the shunt resistance R_{Sh} affects the current flow at low forward voltages and more importantly

the reverse characteristics of diodes with high Schottky barrier height. On the other hand, the parasitic series resistance R_S changes the I-V characteristics, mostly at high voltages [60, 61]. Therefore, using the equivalent circuit illustrated in Fig. 4.4, the diode characteristics can be described by

$$I = I_F - I_R = I_0 \left[\exp\left(\frac{q(V - R_S(T) \cdot I)}{k_B T} \right) - 1 \right] + \frac{V - R_S(T) \cdot I}{R_{Sh}} \tag{4.9}$$

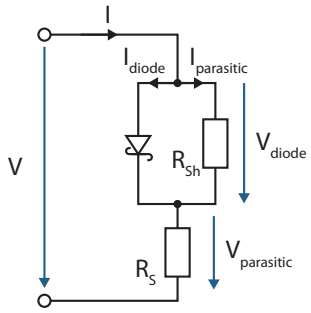

Figure 4.4: Equivalent circuit of a Schottky diode, including series R_S and shunt resistances R_{Sh}.

Interface states

In general, the Schottky barrier is not only determined by the work function difference between the metal and the semiconductor as shown in Equation 4.1, but also by interface states. These energy levels, located within the bandgap of a non-ideal Schottky contact, tend to pin the semiconductor Fermi level at the surface. Their origin are wave functions of the metal's electrons tail which penetrate into the semiconductor in the energy range where the metal conduction band overlaps the semiconductor band gap. These so-called metal-induced gap states (MIGS) change the potential distribution at the interface depending on their density. Interface states can be described by a neutral level $q\Phi_0$ which is located in the band gap. Above $q\Phi_0$ the states are acceptor-like, otherwise they are donor-like. If the bands are bend upwards as described in Chapter 4.1, the charge neutrality level might overcome the Fermi level. In this case, the interface states behave like donors, resulting in a smaller band bending. If the charge neutrality level drops below the Fermi level the interface states behave like donors and increase the band bending. As a result, the Fermi level at the interface is pinned by the surface states close to the neutral level and the barrier height becomes independent

of the work function difference:

$$q\Phi_{Bn}^{0} = E_g - q\Phi_0 \tag{4.10}$$

This description is only valid for Schottky diodes with a very high interface state density ($D_{it} \rightarrow \infty$). For metals on silicon, the Schottky barrier is determined by the workfunction as well as the interface states.

Image-Force Lowering

An electron which is injected from the metal into the semiconductor induces a positive image charge on the metal surface. The resulting attractive image force between the electron and the equal positive image charge is proportional to $1/x^2$, where x is the distance of the electron from the surface. In the presence of an external electric field E_M, the total electron energy $E(x)$ is given by

$$E(x) = -\frac{q^2}{16\pi\varepsilon_{Si}x} - qE_M x \tag{4.11}$$

The image-force lowering $\Delta\Phi$ is then given by the maximum of Equation 4.11, i. e., $dE/dx = 0$, or

$$\Delta\Phi = \sqrt{\frac{qE_M}{4\pi\varepsilon_{Si}}} = \left[\frac{q^3 N}{8\pi^2\varepsilon_{Si}^3}\left(\Phi_{Bn}^{0} - \Phi_{CF} + V\right)\right]^{1/4} \tag{4.12}$$

Equation 4.12 shows, that barrier lowering depends on the doping concentration N of the semiconductor, the difference between the conduction band edge and the Fermi level of the semiconductor Φ_{CF} and more importantly on the applied bias. Fig. 4.5 shows the energy-band diagram of a Schottky contact with image-force induced barrier lowering under different bias conditions.

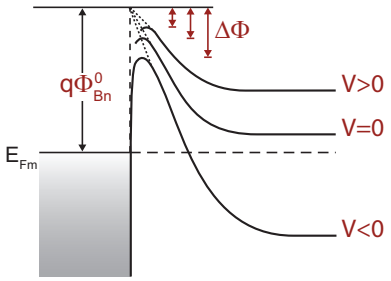

Figure 4.5: Energy-band diagram of a Schottky contact with image force induced barrier lowering under different bias conditions.

Tunneling

As mentioned before, quantum-mechanical tunneling becomes significant for highly doped semiconductors and at low temperatures. A good estimation of the tunneling current can be obtained using the Wentzel-Kramers-Brillouin (WKB) approximation for calculating the reverse current of Schottky diodes (cf. Chapter 4.5.2). A much easier way which is often used is the incorporation of an ideality factor n, which modifies the voltage dependency of Equation 4.7 to $\exp\left(\frac{qV}{nk_BT}\right)$. A strong drawback is that the ideality factor is only defined for forward bias which is less affected by tunneling.

4.5 Extraction of the Schottky Barrier Height

For the extraction of Schottky barrier heights different techniques are usually employed. Widely used are the capacitance-voltage [62], the current-voltage [63], the activation energy [24, 64, 65] and the photoelectric method [66]. However, the most suitable for the used test structures remains the activation energy technique since it is independent of the electrically active area and it can be applied for diodes with very low Schottky barrier heights [67]. Being independent of the mask designed area is very attractive to study silicide-semiconductor interfaces because the electrical surface of carrier injection can be different from this area. The method is more accurate in comparision to other methods because of the use of a two-dimensional data set, $I(V,T)$, for the calculation of Schottky barrier heights [68].

4.5.1 The Arrhenius Plot

Since the activation energy technique is used for the extraction of the Schottky barrier heights of NiSi/Si diodes it is described in more detail here. The underlying Arrhenius plot which is used for the extraction of the Schottky barrier height is a plot of $\ln(I/T^2)$ versus $1/T$ at constant applied forward or reverse voltages. Assuming that the parasitic resistances can be negleted, the thermionic emission theory (Equation 4.7) can be applied. Thus, the Arrhenius plot results in simple linear equations describing the electrical characteristics of the diodes:

$$\ln\left|\frac{I_R}{T^2}\right| = \ln AA^* - \frac{1}{T}\cdot\frac{q\Phi_B^0}{k_B} \qquad \text{for} \qquad \text{V} < 0 \tag{4.13}$$

$$\ln\left|\frac{I_F}{T^2}\right| = \ln AA^* - \frac{1}{T}\cdot\frac{q\left(\Phi_B^0 + n^{-1}V\right)}{k_B} \qquad \text{for} \qquad \text{V} > 0 \tag{4.14}$$

Both equations imply that the Arrhenius plot give a straight line and that the Schottky barrier height can easily be extracted from their slope. However, the series resistance as well as the shunt resistance deteriorate this ideal behavior. Fig. 4.6 illustrates the impact of the parasitics on the shape of the Arrhenius plot. In general, the plot can be divided into three parts, that are the ohmic, the transition and the rectifying region. The ohmic region refers to low Schottky barrier heights or high forward voltages (Fig. 4.6-blue region). Here, the current is limited by the parasitic series resistance. The rectifying region exists for high Schottky barriers and low temperatures where the shunt conductance dominates the low current flow (Fig. 4.6-red region). The region of interest is the transition region lying between the ohmic and the rectifying part (Fig. 4.6-green region). In this region, the influence of both parasitic resistances can be neglected and the expected linear diode behavior is observed. The arrows in Fig. 4.6 indicate the change of the curve shape when the corresponding parameters are altered.

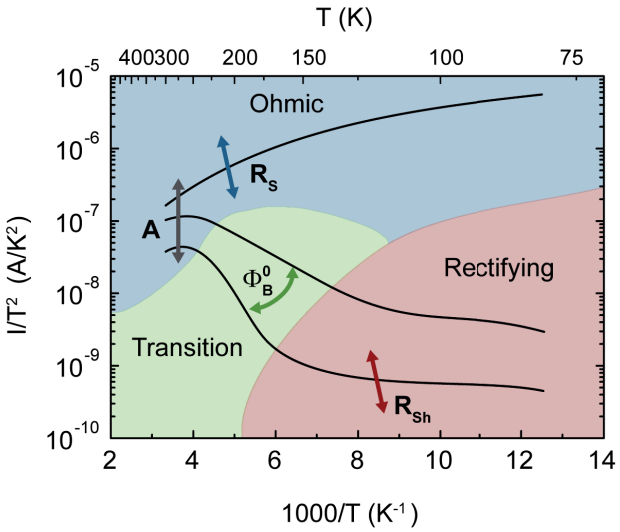

Figure 4.6: Arrhenius plot of a Schottky diode including series and shunt resistances. The ohmic, transition and rectifying regions can be clearly distinguished. The arrows indicate the reshaping of the Arrhenius plot when the corresponding parameters are changed.

4.5.2 Thermionic Emission Theory combined with Tunneling

As already discussed in Chapter 4.4 the real I-V characteristics of Schottky diodes might show strong deviations from the ideal case, not only due to the parasitic resistances. Therefore, the transport model presented by Equation 4.7 has to be extended for an exact extraction of the Schottky barrier height. Extra current flow caused by tunneling and image-force induced barrier lowering has to be incorporated. The approach by Crowell and Rideout offers the advantage of a smooth transition from pure thermionic emission to pure tunneling transport [69]. If Maxwell-Boltzmann statistics is assumed, the net current flow I_R in reverse direction is due to the tails of thermally excited distributions of carriers given by

$$I_R = \frac{AA^*T}{k_B} \int_0^\infty p_m(E)\tau(E)dE \tag{4.15}$$

where $p_m(E)$ is the Boltzmann distribution for states in the metal and $\tau(E)$ is the transmission probability of the Schottky barrier. The Boltzmann distribution $p_s(E)$ of the semiconductor is given by

$$p_s(E) = \exp\left(-\frac{q\Phi_{CF} + E}{k_B T}\right) = p_m(E) \exp\left(\frac{qV}{k_B T}\right) \tag{4.16}$$

Using the WKB approximation [24] and assuming a triangular shape of the Schottky barrier for carriers with an effctive mass m^* and an energy E which is less than the potential energy barrier E_b (cf. Fig. 4.7), the transmission probability is

$$\tau(E) = \exp\left[-\frac{4\pi}{h} \int_{x_0}^{w} \left[2m^* \left(qV(x') - E\right)\right]^{1/2} dx'\right] \tag{4.17}$$

Tunneling occurs in the interval from x_0 to w where $qV(x_0) = E$ and $qV(w) = E_b$ (Fig. 4.7). For thermionic emission, i. e., $E > E_b$, $\tau(E)$ is assumed to be unity. Transformation of Equation 4.17 from an integration over distance into an integral over energy, $\alpha \equiv E/E_b$, results in a reverse current of

$$I_R = I_0 \left[1 + \frac{E_b}{k_B T} \int_0^1 \exp\left(-\frac{E_b}{k_B T}\left[\alpha - 1 + \frac{k_B T}{E_{00}} y(\alpha)\right]\right) d\alpha\right] \tag{4.18}$$

with

$$I_0 = AA^*T^2 \exp\left(\frac{-q\Phi_B^0}{k_B T}\right) \tag{4.19}$$

I_0 is the reverse saturation current of pure thermionic emission, as indicated in Equation 4.6. $E_b = q(\Phi_B^0 - \Phi_{CF} + V_R)$ is the band bending in the semiconductor depletion region, shown in Fig. 4.7. E_{00} is a material constant, associated with the WKB approximation

$$E_{00} = \frac{qh}{4\pi} \left[\frac{N}{m^* \varepsilon_{Si}}\right]^{1/2} \tag{4.20}$$

The ratio of k_BT/E_{00} gives a measure of the dominant current flow. If $k_BT/E_{00} \approx 1$ tunneling dominates whereas for $k_BT/E_{00} \gg 1$ thermionic emission is the dominant transport mechanism. Finally, $y(\alpha)$ is a result of the integral transformation and is defined by

$$y(\alpha) = (1-\alpha)^{1/2} - \alpha \ln\left[\frac{1+(1-\alpha)^{1/2}}{\alpha^{1/2}}\right] \tag{4.21}$$

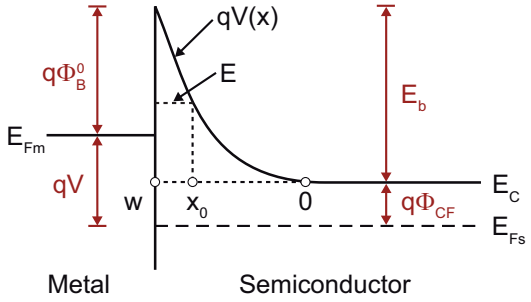

Figure 4.7: Potential energy versus distance for carriers in a reverse biased Schottky diode.

Fig. 4.8 highlights the strong increase of the reverse current I_R as a function of the normalized band bending at the Schottky interface E_b/k_BT for different ratios of k_BT/E_{00}. A current enhancement of several orders of magnitude occurs for the tansition from pure thermionic emission to tunneling injection as dominant transport mechanism.

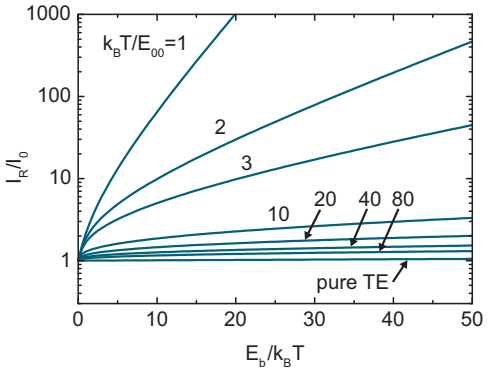

Figure 4.8: Normalized reverse current I_R/I_0 as function of the normalized band bending E_b/k_BT. For $k_BT/E_{00} = 1$ tunneling dominates, whereas a large ratio of k_BT/E_{00} indicates that the current flow is governed by thermionic emission.

4.5.3 Model Application and Validation

To validate the accuracy of the presented model, Equation 4.9 has to be modified for the reverse current and solved numerically as a function of voltage and temperature. A Matlab script is programmed, which allows for a separation of the effects induced by thermionic emission, tunneling and image force induced barrier lowering. The model is then applied to a Schottky diode with a NiSi/p-Si contact, fabricated like described in Chapter 4.6. The series resistance can be extracted from the forward biased diode for high voltages as a function of temperature (Fig. 4.9). This temperature dependence gives a good control over the measurement quality since contact problems would give rise to scattering of R_S.

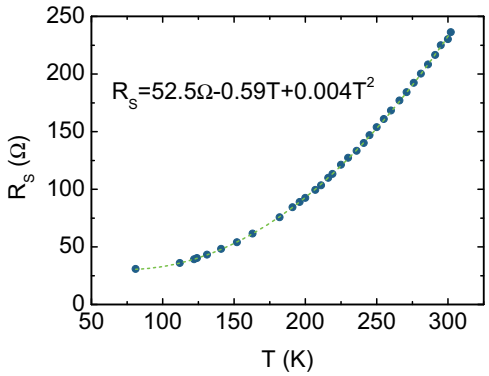

Figure 4.9: Extracted series resistance R_S of a p-type Schottky diode, fabricated like described in Chapter 4.6, as a function of temperature.

Fig. 4.10 presents a comparision of the simulated (solid lines) and measured (dots) reverse Arrhenius plots (I/T^2 vs. $1/T$). It is worth noting that the applied transport model has only three parameters for fitting when the series resistance is directly extracted from the measurements, i. e., the Schottky barrier height Φ_B^0, the shunt resistance R_{Sh} and the doping concentration N at the silicide/silicon interface. The latter can be different from the substrate doping due to dopant segregation and outdiffusion effects [67].

If only thermionic emission is accounted for in the calculation, we observe no voltage dependence of the linear part of the Arrhenius plot for the numerical calculation unlike for the measurement data (Fig. 4.10(a)). Moreover, apart from a good match of the slope in the Arrhenius plot between 260 K and 300 K the calculation and the measurement do not match in the linear part. The voltage-dependent effect of the shunt resistance can be seen for temperatures smaller than 240 K as a saturation of

the curves. Including image force induced barrier lowering as described in Chapter 4.4, Fig. 4.10(b), as well as tunneling, Fig. 4.10(c), results in both cases in a voltage dependence of the Arrhenius plots. An excellent agreement between the measurement data and the calculation is only achieved, when all effects are included in the simulation, as demonstrated in Fig. 4.10(d). Here, the optimal parameters are $N = 3.2 \cdot 10^{15}\,\mathrm{cm}^{-3}$, $R_P = 3.2 \cdot 10^5\,\Omega$ and a Schottky barrier height for holes of $\Phi^0_{Bp} = 0.455\,\mathrm{eV}$. This Schottky barrier height of a NiSi/p-Si contact agrees very well with literature data [70]. The boron concentration at the NiSi/Si interface is slightly higher than expected for a wafer with a specification of $7-21\,\Omega\mathrm{cm}$ ($\approx 2 \cdot 10^{15}\,\mathrm{B/cm}^2$), which can be explained by dopant segregation.

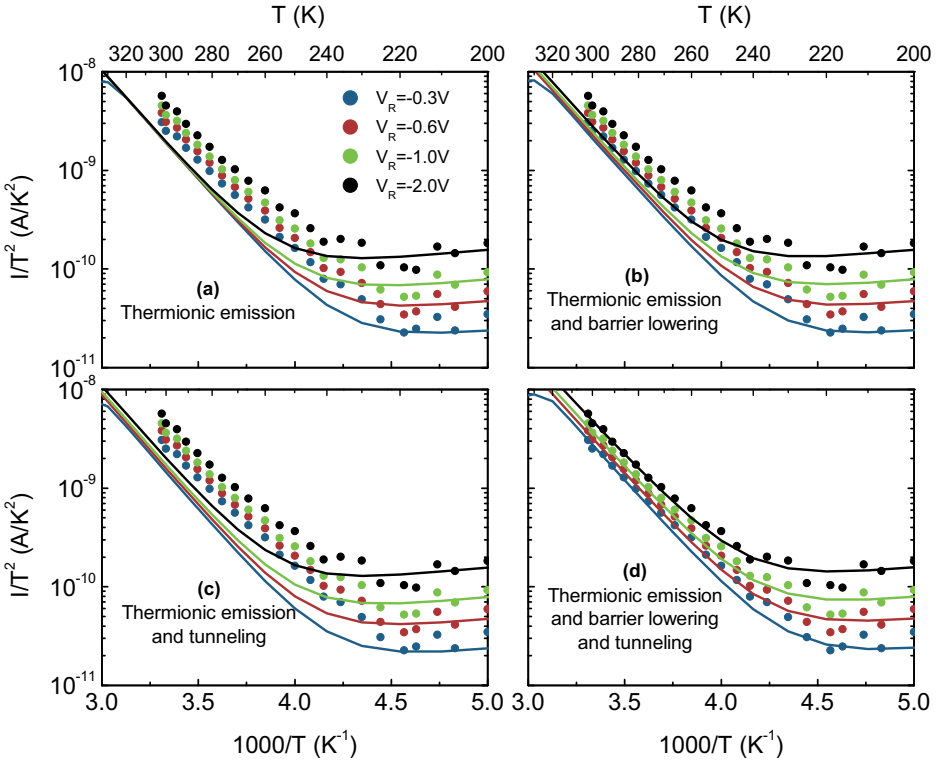

Figure 4.10: Experimental (dots) and calculated (solid lines) reverse-current Arrhenius plots using the following models: (a) Pure thermionic emission. (b) Thermionic emission and barrier lowering. (c) Thermionic emission and tunneling. (d) Thermionic emission including barrier lowering and tunneling. The model parameters are: $\Phi^0_{Bp} = 0.455\,\mathrm{eV}$, $N = 3.2 \cdot 10^{15}\,\mathrm{cm}^{-3}$, $R_P = 3.2 \cdot 10^5\,\Omega$.

Fig. 4.11 shows a good agreement of the calculation and the measurement for the forward Arrhenius plot, too. Here, we observe a deviation for small applied voltages (+0.1 V and +0.3 V) since only thermionic emission combined with image force induced barrier lowering are included in the calculation of the forward current. For larger forward bias, the tunneling mechanism becomes less important and does not affect the Arrhenius plot anymore. In fact, the current gets more and more limited by the series resistance.

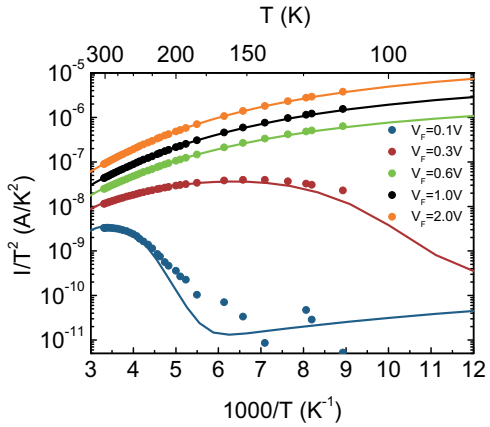

Figure 4.11: Calculation (solid lines) and experimental data (dots) of the forward Arrhenius plot.

4.6 Fabrication of SB-Diodes

For the fabrication of NiSi Schottky diodes with and without dopant segregation, n-type and p-type bulk silicon (100) wafers with resistivities of 1-8 Ωcm and 7-21 Ωcm are used, respectively. A high dose of $3{\cdot}10^{15}$at/cm^2 As^+/B^+ ions at energies of 115 keV/20 keV is implanted into the backside of the Si substrate for the formation of an ohmic contact. The dopant activation occurs during wet oxidation at a temperature of 1050°C which results in 300 nm thermal SiO_2. The diode areas are defined by patterning the SiO_2 on the front side of the wafer by optical lithography and reactive ion etching (RIE) using a CHF_3 plasma, followed by ion implantation. To study the impact of dopant segregation Schottky diodes with B^+, As^+ and Sb^+ implantation are fabricated. The chosen implantation conditions, which are shown in Table 4.1, result in an implantation depth of approximately 8 nm which is first simulated with the program SRIM and then confirmed using secondary ion mass spectrometry (SIMS). The Schottky diodes are

treated in different ways prior to silicidation induced dopant segregation in order to compare the effects of thermally activated versus non activated dopants. Therefore, for one half of the samples the dopants are activated by a 1000°C spike-annealing step in a rapid thermal processing furnace (RTP) prior to silicidation. After a standard cleaning the native oxide is etched directly before Ni deposition. The Ni thickness is chosen in a way that ensures a complete consumption of the ion implanted area during silicidation. For a comparison of the Schottky barrier heights, standard diodes are also fabricated on unimplanted Si. The silicidation is carried out in an RTP system in forming gas (90% N_2 + 10% H_2) for 90 s at a temperature of 500°C, where no dopant activation and diffusion occurs. The unreacted Ni is then selectively wet etched using sulfuric acid-hydrogen peroxide mixture (SPM) with 4 parts H_2SO_4 and 1 part H_2O_2. Finally, the oxide at the backside is wet etched by 10% buffered hydrogen fluoride (HF) while protecting the front side of the wafer with resist and aluminum is deposited on the highly doped backsides of the wafers, providing ohmic back contacts for the diodes.

Dopant	**Energy (keV)**	**Dose (at/cm^2)**
As^+	5	$5{\cdot}10^{13}$ - $1{\cdot}10^{15}$
B^+	2	$5{\cdot}10^{13}$ - $1{\cdot}10^{15}$
Sb^+	6	$1{\cdot}10^{14}$ - $5{\cdot}10^{15}$

Table 4.1: Implantation conditions for Schottky diodes with dopant segregation.

4.7 Temperature-Dependent Measurements

To perform temperature-dependent measurements, a vacuum chamber setup is used which can be evacuated down to 10^{-4} mbar by a turbomolecular pump. The samples are glued with conductive silver paste on a cooling head where four probe heads with tungsten needles are arranged circular around it for electrical contacting of the devices. A thermocouple in combination with a proportional, integral, derivative (PID) controller and a heater allows an exact temperature control and facilitates measurements from 77 K using liquid nitrogen up to 470 K. Heating beyond room temperature is of great importance for the extraction of high Schottky barrier heights. The measurements are made using an HP 4155B semiconductor parameter analyzer and a dedicated software.

4.8 NiSi/p-Si Contacts with B Segregation

Fig. 4.12 shows the current-voltage characteristics of NiSi/p-Si Schottky diodes with and without B segregation at room temperature. Diodes with boron implantation show much higher reverse saturation currents compared with pure NiSi/Si contacts which indicates Schottky barrier lowering due to silicidation induced dopant segregation. At an implantation dose of $5{\cdot}10^{14}$ B/cm^2 ohmic contact behavior with equal currents for positive and negative voltages is observed.

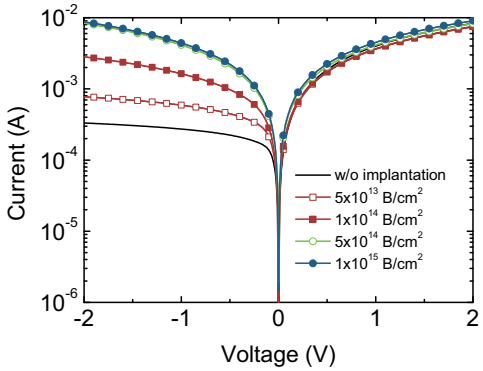

Figure 4.12: *I-V* characteristics of NiSi/p-Si (100) with and without B segregation.

Since the numerical calculation of the model presented before is very time-consuming, here a quantitative analysis is performed by extraction of the barrier heights for holes at different voltages using the pure thermionic emission theory. Fig. 4.13 shows the extracted barrier heights for diodes with different implantation dose versus the applied voltage. Then, the Schottky barrier heights are extrapolated in the limit of zero applied bias [9] where image-force induced barrier lowering as well as tunneling, which both result in a voltage dependency, should not affect the extracted values. However, it is found, that this technique does not provide the real Schottky barrier height as the thermionic emission theory combined with barrier lowering and tunneling, but an effective Schottky barrier height $\Phi_{B,eff}$ (eSBH). The lower of values $\Phi_{B,eff}$ are a result of disregarding image-force induced barrier lowering which is even without any applied bias apparent and of tunneling which changes the slope of the Arrhenius plot not only in voltage dependence, but also in temperature dependence. Nevertheless, this technique gives a good measure of the efficiency of carrier injection of Schottky contacts. Fig. 4.14 shows the effective Schottky barrier heights for holes as a function of the implantation

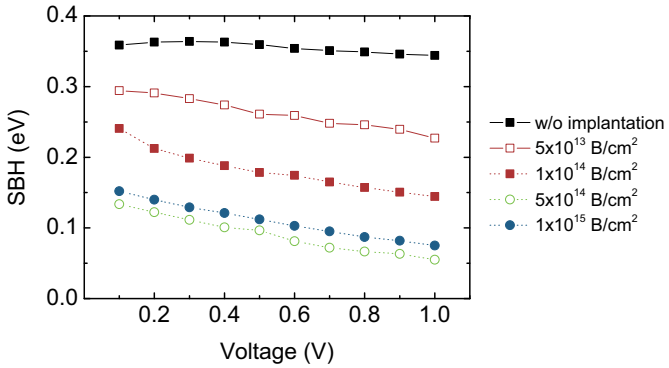

Figure 4.13: Schottky barrier heights (SBH) at different reverse voltages for NiSi/p-Si Schottky diodes with and without dopant segregation.

dose. A reduction from $\Phi_{B,eff} = 0.36\,\text{eV}$ without implantation to $\Phi_{B,eff} = 0.13\,\text{eV}$ for a dose of $1{\cdot}10^{15}$ B/cm^2 is observed. Fig. 4.14 also shows the impact of dopant activation prior to silicidation. An activation of the dopants, using spike-annealing at 1000°C before silicidation, leads to even lower eSBHs in the sub-0.1 eV regime when a dose larger than $5{\cdot}10^{14}$ B/cm^2 is used. These lower values indicate that a larger amount of dopants is activated at the silicide/silicon interface after dopant segregation.

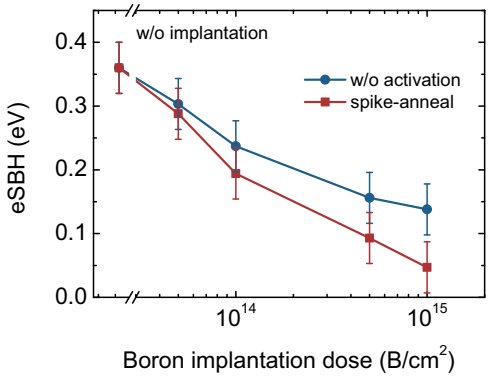

Figure 4.14: Extracted effective Schottky barrier heights in the limit of zero applied bias for different boron implantation doses. Lower values are achieved when the dopants are activated prior to silicidation.

The dopant depth-profiles of the diodes are measured with time-of-flight secondary-ion mass spectrometry (TOF-SIMS) using a 2 keV O_2-ion-beam. For calibration of the measurements two standards with known boron concentrations are used, a B-

implanted Si wafer and a wafer with a thick B-implanted NiSi layer. Fig. 4.15 shows the expected pile-up of B dopants at the NiSi/Si interface around 120 nm depth. One should note, that the original implantation depth is around 8 nm. The B concentration peak at the NiSi/Si interface which is far below the implantation depth is therefore caused by dopant segregation due to the snow-plow effect (cf. Chapter 3.3). The peak concentration at the interface shows a strong dose dependence and reaches a value of $1.3{\cdot}10^{19}\,\mathrm{B/cm^3}$ for the highest dose of $1{\cdot}10^{15}\,\mathrm{B/cm^2}$. The broadening of the SIMS profile is related to the NiSi surface and interface roughness as well as to the SIMS depth resolution.

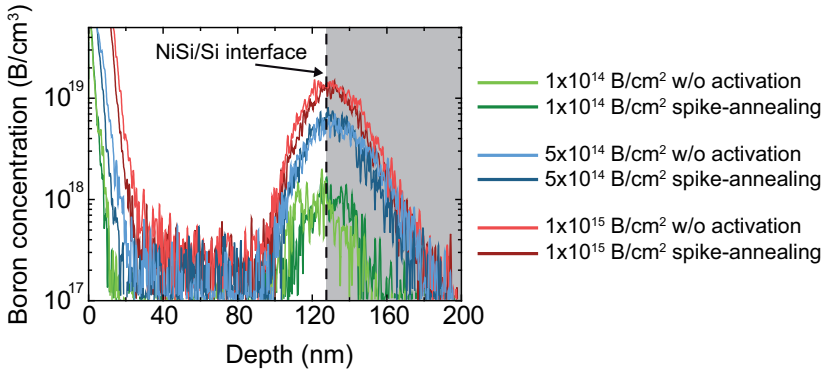

Figure 4.15: SIMS depth profiles of NiSi/p-Si Schottky diodes for various B implantation doses with activated and non-activated dopants prior to silicidation.

4.9 NiSi/n-Si Contacts with As Segregation

Besides the investigation of boron segregation to lower the effective barrier height for holes, NiSi/n-Si diodes with arsenic segregation are characterized. Fig. 4.16 shows the *I-V* characteristics of diodes without and with dopant segregation using different arsenic doses. An ohmic contact behavior is already observed for the low implantation dose of $1{\cdot}10^{14}\,\mathrm{As/cm^2}$. According to the *I-V* characteristics, a drastic decrease of the effective Schottky barrier height for electrons can be observed even for the lowest implantation dose. Diodes with dopants not activated before silicidation show a minimum eSBH of $\Phi_{B,eff} = 0.13\,\mathrm{eV}$ for an implantation dose of $1{\cdot}10^{15}\,\mathrm{As/cm^2}$ (see Fig. 4.17). For higher implantation doses the eSBH rises again, which might be due to deactivation of dopants at the NiSi/Si interface [71]. An activation of the dopants prior to Ni deposition leads to lower effective barrier heights. On average, dopant activation reduces the

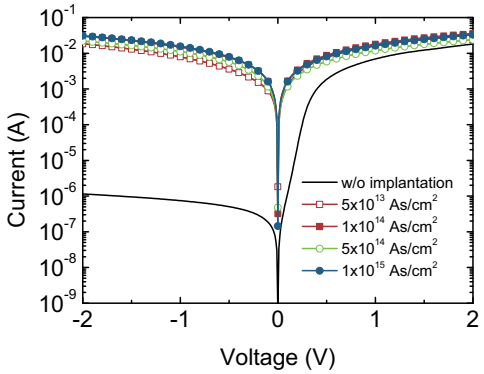

Figure 4.16: *I-V* characteristics of NiSi/n-Si (100) Schottky diodes with and without arsenic segregation.

eSBH remarkably by about 34%. The corresponding SIMS measurements (Fig. 4.18), performed using a 2 keV Cs-ion-beam, show the expected pile-up of As dopants as was already observed for boron segregation. Here, a broader pile-up peak, $d_{Pile-up}$ is observed for samples with activation of dopants prior to silicidation. Besides a larger amount of activated dopants at the NiSi/Si interface, we assume that this broader distribution induces an additional lowering of the eSBH, due to $\Delta\Phi_B \propto d_{Pile-up}^{1/2}$ [72].

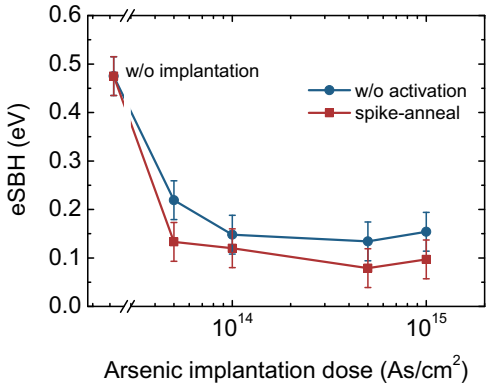

Figure 4.17: Effective SBH's for different As implantation doses showing lower $\Phi_{B,eff}$ for diodes with dopants which are activated prior to silicidation.

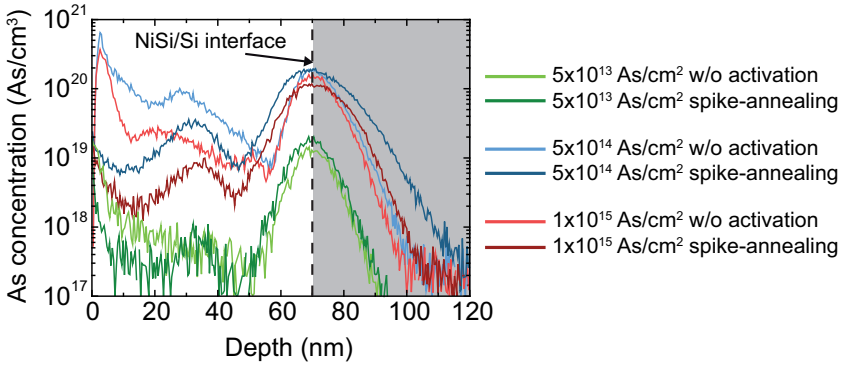

Figure 4.18: SIMS depth profiles showing As segregation at the NiSi/Si interface for three different arsenic implantation doses.

4.10 NiSi/n-Si Contacts with Sb Segregation

As alternative for As segregation to lower the eSBH for electrons, diodes with Sb implantation are investigated. Fig. 4.19(a) shows the current-voltage characteristics of the NiSi Schottky diodes formed on Sb implanted n-Si(100). As already observed for B and As, all doped diodes show higher reverse saturation currents compared to the pure NiSi/Si Schottky diode without ion implantation. Therefore, the extracted eSBH's in Fig. 4.19(b) show distinct barrier lowering depending on the dopant concentration. The eSBH is reduced from 0.48 eV for the pure NiSi/Si contact without dopant segregation to 0.13 eV for the highest Sb implantation dose of $5{\cdot}10^{15}$ Sb/cm^2. This value is comparable to the extracted effective SBH of 0.13 eV for As segregation with a much lower implantation dose of $5{\cdot}10^{14}$ As/cm^2. The SIMS depth profiles of the Sb diodes, presented in Fig. 4.20, show the expected dose-dependent pile-up of Sb at the NiSi/Si interface. The biggest pile-up concentration, $1{\cdot}10^{20}$ Sb/cm^3, is achieved for the highest measured implantation dose of $1{\cdot}10^{15}$ As/cm^2. Though, this value is comparable to the peak concentration of diodes with As segregation, we should note, that the segregation length is smaller in case of the Sb diodes. Here, the resulting NiSi layer has a thickness of around 39 nm instead of 70 nm which is the case for the As diodes. If a 65 nm thick NiSi layer is used for antimony segregation, the pile-up concentration of Sb is strongly reduced by 70% in comparison to the 39 nm thick NiSi layer.

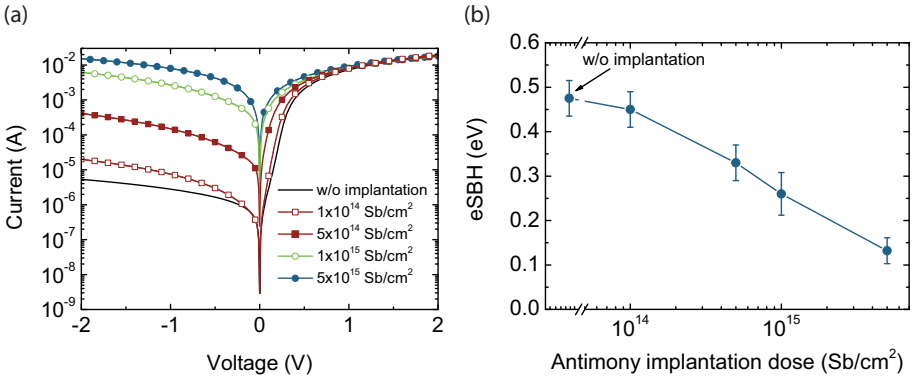

Figure 4.19: (a) Current-voltage characteristics of NiSi/n-Si(100) Schottky diodes without ion implantation and with Sb segregation using different implantation doses. (b) Extracted effective SBH of NiSi on n-type Si(100) as a function of the implanted Sb dose. The minimum effective SBH of 0.13 eV is achieved at a dose of $5{\cdot}10^{15}$ Sb/cm^2.

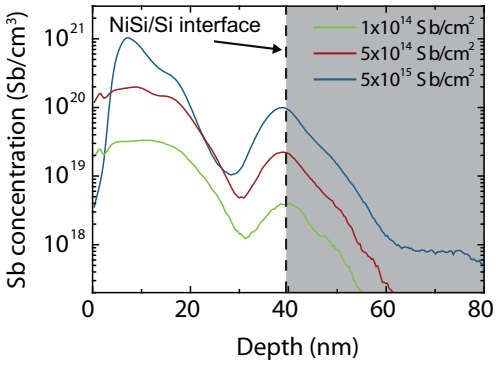

Figure 4.20: SIMS depth profiles of antimony after silicidation showing the dopant pile-up for various implantation doses at the NiSi/Si interface.

4.11 Summary

In summary, NiSi Schottky diodes using silicidation induced dopant segregation are fabricated and electrically characterized by performing temperature-dependent measurements. The proposed physical transport model for Schottky contacts that accounts for thermionic emission in combination with barrier lowering and tunneling provides a perfect agreement between the calculated and measured reverse Arrhenius plots of

NiSi/p-Si Schottky contacts. The I-V characteristics of diodes with dopant segregation exhibit much higher reverse saturation currents than of diodes without ion implantation which indicates lower Schottky barrier heights. A quantitative analysis of these diodes is done by extrapolating the effective Schottky barrier heights at zero-applied bias which provides a good measure of the efficiency of carrier injection through metal-semiconductor contacts. Effective Schottky barrier heights in the order of 0.1 eV are obtained for holes and electrons using B and As or Sb segregation, respectively. An activation of the dopants results in even lower eSBHs in the sub-0.1 eV regime, indicating a larger amount of activated dopants at the NiSi/Si interface. SIMS measurements show the expected pile-up of dopants at the NiSi/Si interface which is strongly dependent on the implantation dose and reflects the dose dependence of the eSBH.
Fig. 4.21 compares the effective Schottky barrier heights of the fabricated Schottky diodes with literature data [9–11, 17, 67, 73, 74]. Amazing is the feasibility of tuning the barrier height of NiSi for electrons as well as for holes to approximately 0.1 eV, below which the Schottky S/D architecture favorably competes with conventional MOSFETs [7, 8]. Besides dopant segregation, using different impurity atoms, a low Schottky barrier for electrons can also be obtained by using rare earth silicides like ErSi [10] and YbSi [11] or combining Er with Pt [9]. The use of PtSi in combination with boron segregation [17, 67] results in similar barrier heights for holes as for the presented NiSi/p-Si Schottky diodes.

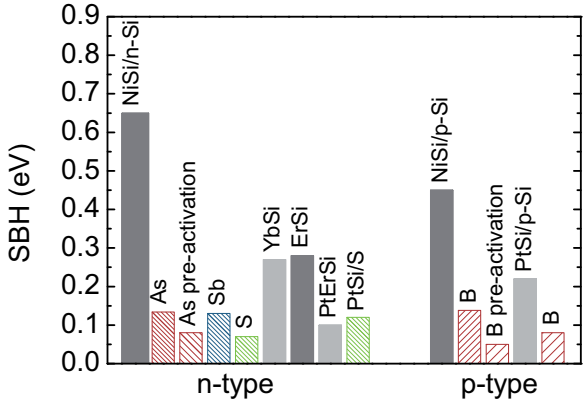

Figure 4.21: Comparison of extracted Schottky barrier heights for electrons (n-type) [9–11, 73, 74] and for holes (p-type) [17, 67].

Chapter 5

Fabrication Process of SB-MOSFETs

The mask layout and fabrication process of NiSi source/drain SB-MOSFETs on thin-body SOI are described in the following sections. The emphasis is put on key process steps with focus on the fabrication of short-channel devices.

5.1 Mask Design

Fig. 5.1 shows the mask layout for samples with a size of $22{\cdot}22\,\mathrm{mm}^2$ which contains the MOSFETs, different test structures and various control fields for processing. The outer border lines with crosses in the edges which become successively smaller with each process step deal as alignment markers for the optical lithography, whereas $15{\cdot}15\,\mu\mathrm{m}^2$ large squares are used as markers for electron-beam (e-beam) lithography. The two large squares in the upper left corner which contain arrays of e-beam markers are so-called pre-allocation markers (PAM) which simplify the adjustment of the samples during e-beam writing. The two squares on the right side of the PAM fields allow a control of each process step either by laser interferometry during dry etching or by spectroscopic ellipsometry. The upper field contains the whole layer stack, including the SOI substrate, the gate oxide and the gate stack, whereas the lower field is etched down to the substrate. This is especially important for the SiO_2 spacer etching since in-situ laser interferometry during etching does not show any etch-stop signal on thin SOI layers. The rectangle on the right side serves as control field and provides test structures for TEM.
In the lower part each of the four areas, devided by alignment lines, contains $6 \cdot 8 \cdot$

2 MOSFETs with two gate-fingers. The gate lengths vary between $L_g = 80\,\text{nm}$ to 380 nm for two different gate widths of $W_g = 2{\cdot}40\,\mu\text{m}$ and $2{\cdot}100\,\mu\text{m}$ in case of the short-channel SB-MOSFETs. In the upper part between the control fields dedicated test structures, such as open's for the two different gate widths, transmission-line-model (TLM) structures, gated hallbars with four widths of 20 to $80\,\mu\text{m}$ and back-to-back Schottky diodes with 25 to $200\,\mu\text{m}$ widths are placed.

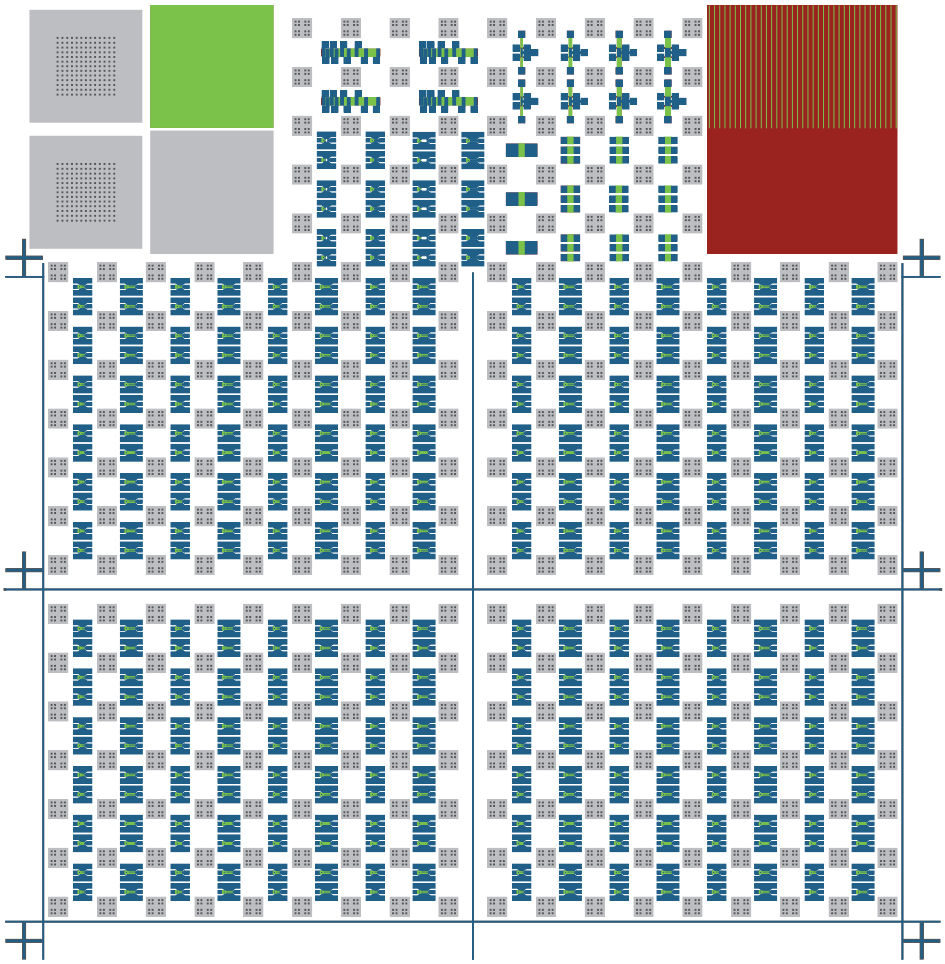

Figure 5.1: Mask layout for the fabrication of the short-channel SB-MOSFETs.

5.2 Layout of SB-MOSFETs

The layout of the thin-body SOI SB-MOSFETs is designed in a way, that it meets the requirements of S-parameter measurements (see Chapter 7.1) while keeping the fabrication as simple as possible in order to obtain a reproducible process. The results are mesa-isolated two-finger SB-MOSFETs with coplanar waveguide (CPW) transmission lines, presented in Fig 5.2. The ground-signal-ground (GSG) layout with 100 μm-pitch is chosen to obtain a perfect shielding of the device [75], see Fig. 5.3, when performing S-parameter measurements. Large gate width's of $W_g = 2{\cdot}40\,\mu$m and $W_g = 2{\cdot}100\,\mu$m for the short-channel devices ensure a large total current flow which is neccessary for the microwave measurements.

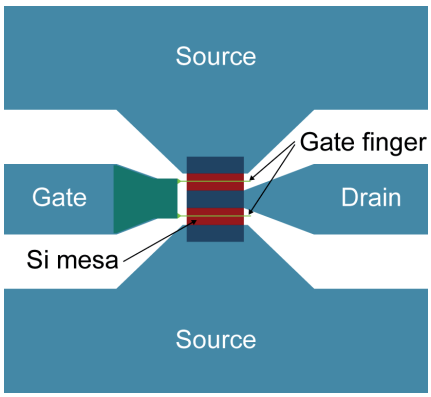

Figure 5.2: Layout of two-finger SB-MOSFET with CPW transmission lines.

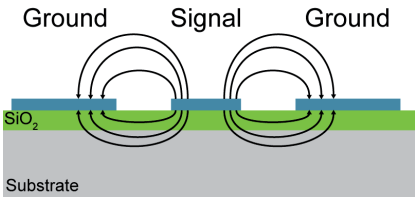

Figure 5.3: Electric field distribution for ground-signal-ground (GSG) transmission lines.

5.3 Fabrication Process

Intrinsic SOI substrates with a thickness of $t_{Si} = 20\,\text{nm}$ and 30 nm are used for the fabrication of the SB-MOSFETs. The buried oxide (BOX) has a thickness of 100 nm which is favourable for the RF analysis because coupling effects through the substrate can be neglected due to the thick insulation layer.
Fig. 5.4 shows a schematic illustration of the key fabrication steps of the SB-MOSFETs while Table 6.1, 6.2 and 6.3 summarize the device dimensions and layer thicknesses for the long- and short-channel SB-MOSFETs.

E-Beam Marker

If short-channel SB-MOSFETs are fabricated, the markers for electron-beam writing have to be patterned by optical lithopgraphy. In a first negative lithography step using AZ 5214 resist, $150{\cdot}150\,\mu\text{m}^2$ large squares, the two PAM fields and the lower process control field are patterned (cf. Fig. 5.1). The SOI layer is then dry etched using reactive ion etching (RIE) with an Ar/SF_6 plasma, followed by RIE-etching of the buried oxide layer down to the substrate using a CHF_3 plasma . An oxygen plasma after each CHF_3 etching is used to remove polymers on the silicon surface.
In a second positive lithography step using UV 6.06 resist, the $15{\cdot}15\,\mu\text{m}^2$ large e-beam markers are etched 800 nm deep into the Si substrate using an Ar/SF_6 plasma.

Mesa Definition

For the electrical insulation of the MOSFETs, Si mesas are defined by positive optical lithography (UV 6.06) and RIE etching. The widths of the mesas are $10\,\mu\text{m}$ to $40\,\mu\text{m}$ for long-channel SB-MOSFETs and $40\,\mu\text{m}$ and $100\,\mu\text{m}$ for short-channel devices, respectively.

Gate stack formation

Directly after RCA cleaning [76], a 3.5 nm (4.5 nm) thick gate oxide is grown by dry oxidation at 800°C for 20 minutes (30 minutes) using a rapid thermal processor (RTP). After oxidation, 160 nm n^+-polycrystalline Si (poly-Si) is deposited by low pressure chemical vapour deposition (LPCVD) followed by an activation of the dopants at 1000°C for 1 minute in an RTP. Depending on the gate patterning by optical or e-beam lithography, a 100 nm thick SiO_2 layer is deposited by LPCVD as hard mask for

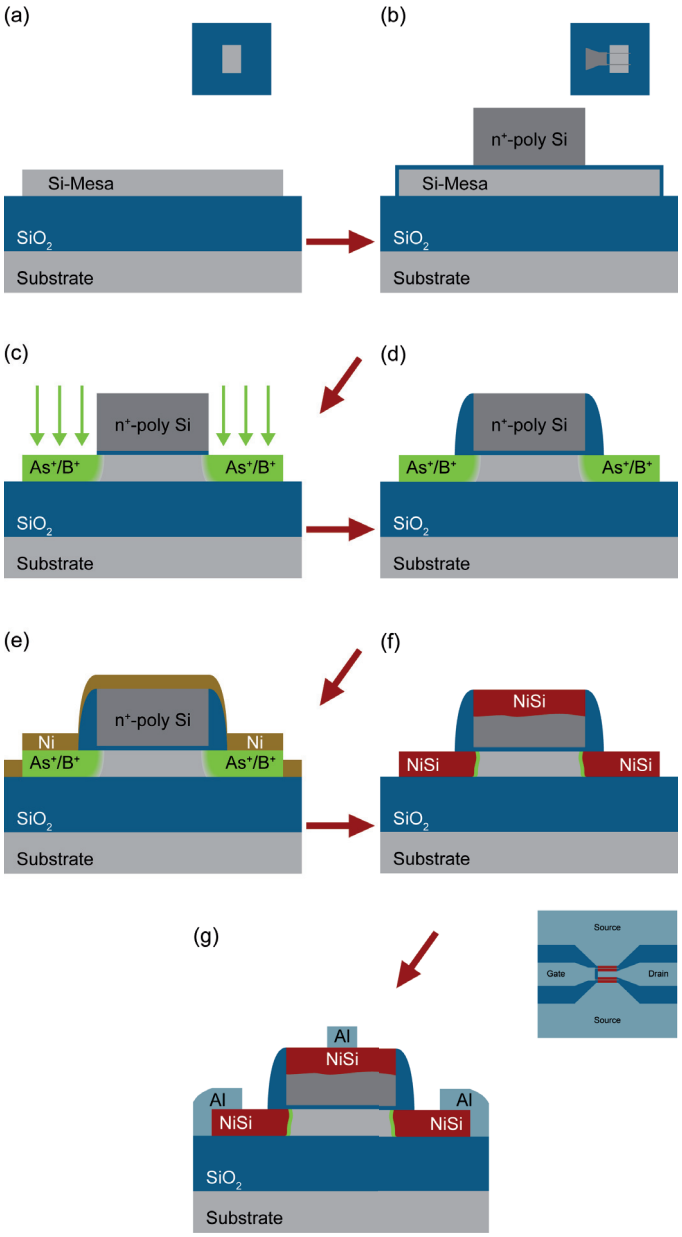

Figure 5.4: Illustration of the key fabrication steps of short channel SB-MOSFETs. (a) Mesa isolation, (b) gate stack formation, (c) ion implantation, (d) spacer formation, (e) Ni deposition, (f) silicidation, (g) metallization.

gate-stack etching or the e-beam resist Hydrogensilsesquioxan (HSQ) is spinned on the poly-Si.
In the case of long-channel devices, the 100 nm SiO_2 on top of the poly-Si is patterned by optical lithography, followed by reactive ion etching (CHF_3). The poly-Si is then structured by inductively coupled plasma etching (ICP-RIE), using the SiO_2 on top of the poly-Si as hard mask and the gate oxide as etch stop layer. In a first step, the native oxide on top of the poly-Si is removed by pure HBr plasma. The high selectivity between Si and SiO_2 of the second step, an $HBr : O_2$ plasma, permits an exact etch stop and steep edges [77]. The resulting gate lengths range from $L_g = 1.0\,\mu$m to $4.0\,\mu$m.
For short-channel SB-MOSFETs, e-beam lithography is used to define the gate stacks with lengths from $L_g = 80$ nm to 380 nm, followed by ICP-etching, too. However, in contrast to the SiO_2 hard mask, the HSQ is completely etched during the ICP-etching which avoids an additional step to open the gate contact windows and facilitates a partial silicidation of the gate stack. Fig. 5.5 shows a scanning electron microscopy (SEM) image of a straigth gate finger ($L_g = 180$ nm) with its steep edges.

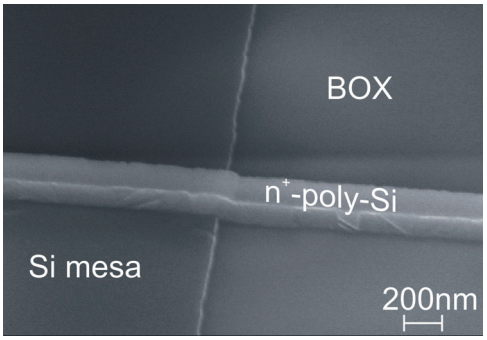

Figure 5.5: SEM image (60° tilted) of the Si mesa of a SB-MOSFET on thin-body SOI ($t_{Si} = 30$ nm) with a 3.5 nm gate oxide and a 160 nm thick n^+-poly-Si gate; the channel length is 180 nm.

Ion Implantation

A wet etching step using 1% HF removes the gate oxide at S/D in order to implant directly into the SOI layer. For SB-MOSFETs with dopant segregation, either B^+ at an energy of 1.5 keV or As^+ at an energy of 5 keV are implanted under a tilt angle of 0°, leading to an implantation depth of approximately 8 nm in both cases. For the B^+ implantation, different doses of $5{\cdot}10^{14}$ B/cm^2, $1{\cdot}10^{15}$ B/cm^2 and $3{\cdot}10^{15}$ B/cm^2 are chosen. For the As^+ implantation doses ranging from $5{\cdot}10^{13}$ As/cm^2 to $6{\cdot}10^{15}$ As/cm^2 are used.

Gate Spacer Formation

After implantation tetra-ethyl-ortho-silicate (TEOS) is deposited by LPCVD which ensures a conformal deposition of SiO_2 and a perfect coverage of the edges. During the following anisotropic dry etching by RIE in a CHF_3 plasma, SiO_2 gate spacers are formed. This step is very critical since the SiO_2 has to be etched away completely while the thin SOI layer serves as etch stop layer. Therefore, a very good selectivity between SiO_2 and Si is mandatory to prevent a loss of the highly doped silicon S/D regions. Whereas the long-channel SB-MOSFETs and the first batch of the short-channel devices are etched with a poor selectivity, a drastically improved CHF_3 process is developed and used for the short-channel devices with different As^+ implantation doses (see Chapter 7.7). Here, a selectivity better than 10 : 1 at an etch rate of 60 nm/min results in improved device characteristics.

Gate Contact Window Opening

Negative Optical lithography (AZ 5206) is used to pattern the gate contact windows in case of long-channel SB-MOSFETs. The SiO_2 hard mask on top of the poly-Si is then etched by RIE.

Silicidation

The samples are then cleaned using SPM ($H_2SO_4 : H_2O_2 = 4 : 1$), and directly after an HF-dip (1%) for 30 s Ni is deposited by electron-beam evaporation. The required Ni thickness strongly depends on t_{Si}. For the subsequent silicidation step, a temperature of 450 °C and a time of 30 seconds are chosen in order to facilitate dopant segregation and the encroachment of NiSi into the channel region as displayed in Fig. 5.6 for a 80 nm short-channel MOSFET. The unreacted Ni is selectively wet etched using SPM. Whereas Fig. 5.6(a) shows a standard SEM image, the bright-field scanning transmission electron microscopy (STEM) image, Fig. 5.6(b), shows a Z-contrast, where heavy atoms like Pt and Ni appear in dark and light atoms in bright colors. The different contrasts of the Pt layers are a result of two deposition techniques.

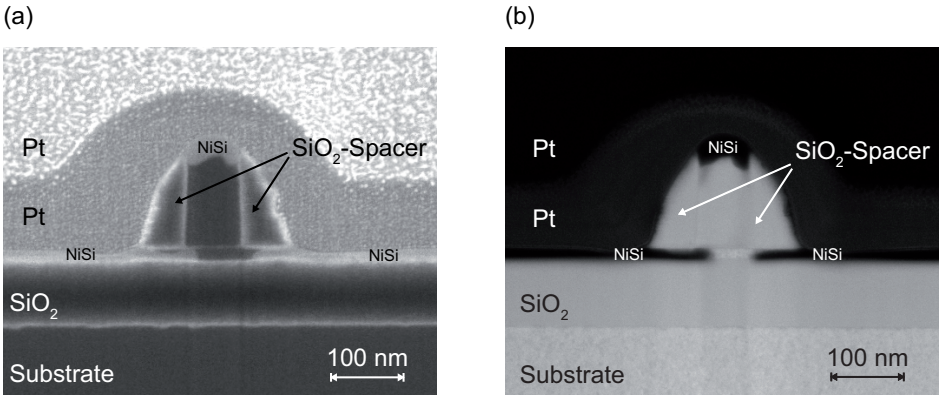

Figure 5.6: (a) SEM and (b) bright-field STEM images of a 80 nm short-channel SB-MOSFET preparated by focused ion beam (FIB), showing the NiSi encroachment under the spacer and the partially silicided gate stack ($t_{Si} = 20$ nm, $t_{ox} = 4.5$ nm).

Metallization of the Contacts

Finally, negative lithography (AZ 5214) is used to pattern the CPW transmission lines of gate, source and drain for lift-off procedure. The native oxide on top of the silicide is removed by 10 to 15 s Ar sputtering, followed by deposition of 20 nm Cr and 200 nm Al. The Cr layer is used for better adhesion of the Al layer on the silicide [71]. Fig. 5.7 shows an SEM image of a readily fabricated device with a gate length of $L_g = 80$ nm and a gate-width of $W_g = 2{\cdot}40\,\mu$m.

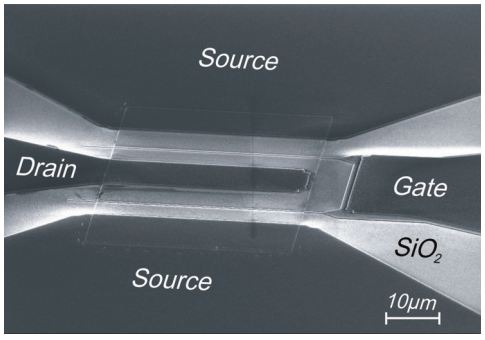

Figure 5.7: SEM image of a two-finger SB-MOSFET with CPW transmission lines on ultra-thin SOI ($t_{Si} = 20$ nm) with a 3.5 nm gate oxide and a 160 nm thick n^+-poly-Si gate. The channel length is 80 nm.

Chapter 6

DC-Characteristics of SB-MOSFETs

This chapter deals with the direct-current (DC) characteristics of Schottky barrier (SB) MOSFETs. After the characterization of the gate-oxide, the operation principle of SB-MOSFETs is examined using the corresponding band diagrams. This highlights the peculiarities of these devices that show a distinct different switching behavior when compared to conventional MOSFETs. Then, the electrical characteristics of SB-MOSFETs with silicidation induced dopant segregation using B or As are discussed for long- and short-channel MOSFETs. Finally, the 80 nm-short channel devices are compared with state-of-the-art SB-MOSFETs.

6.1 Gate Oxide

For the fabrication of MOS capacitors, boron-doped Si(100) wafers are used with a resistivity of 1-10 Ωcm, corresponding to a substrate doping of 10^{15}-10^{16} B/cm^3. After RCA cleaning the samples are oxidized at 800°C for 20 min in an RTP system at a constant oxygen flow. The top contacts are then defined by e-beam evaporation of 200 nm Al through a shadow mask while an ohmic backside contact is realized by deposition of 120 nm Al on the backside of the wafers followed by a drive-in anneal at 400°C for 10 min in a forming gas atmosphere (90% N_2+10% H_2).
The electrical characterization of the capacitors is performed using an HP 4192A impedance analyzer for C-V-measurements and a Keithley 4200 SCS semiconductor characterization system for leakage current measurements. Fig. 6.1 shows nearly perfect C-V-curves of the resulting 3.5 nm thick SiO_2 gate oxide which thickness is determined

by spectroscopic ellipsometry. The inset of Fig. 6.1 presents I-V-curves of different samples which reveal low leakage currents over the whole voltage range. From the capacitance value in accumulation, e.g. at $-2.5\,\mathrm{V}$, the capacitance equivalent thickness (CET) can be calculated. The CET value of 3.1 nm corresponds to the thickness of an ideal SiO_2 with $\varepsilon_{SiO_2} = 3.9$ having the same electrical capacitance as this thermally grown oxide if quantum effects are neglected.

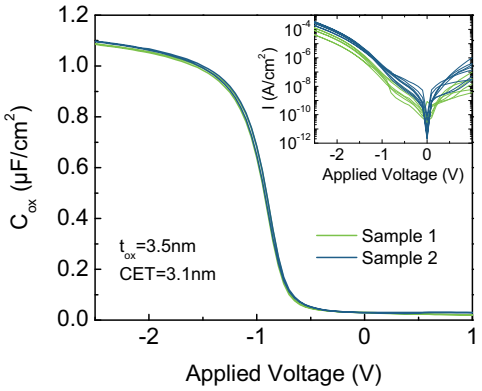

Figure 6.1: C-V curves of the 3.5 nm thick SiO_2 gate oxide. The inset shows the leakage current versus applied voltage.

The interface state densities D_{it} derived from the C-V curves using Termans' method [78, 79] lie around $2 \cdot 10^{11}\,(\mathrm{eVcm}^2)^{-1}$ which is a quite reasonable value for thermally grown SiO_2.

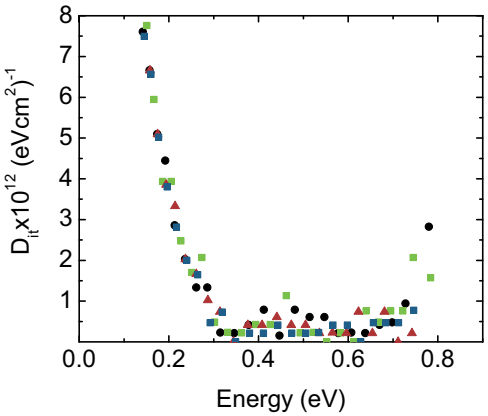

Figure 6.2: Interface state density D_{it} derived from the C-V curves using Termans' method [78] shows a low D_{it} value of $2 \cdot 10^{11}\,(\mathrm{eVcm}^2)^{-1}$.

6.2 Operation Principle of SB-MOSFETs

Since the switching behavior of SB-MOSFETs is different from conventional devices where the current flow is determined by the potential barrier in the channel and not by a modulation of the carrier injection through the contacts, the basic electrical characteristics of SB-MOSFETs are investigated in more detail. A typical transfer characteristic ($I_d - V_{gs}$) of a SB-MOSFET and the corresponding band diagrams are shown in Fig. 6.3 for different bias conditions. Since NiSi is used with an undoped channel for the device fabrication (cf. Chapter 5), a Fermi level which is pinned more closely to the valence band than at midgap and an intrinsic channel are assumed for the schematic band diagrams. If the device with a lower SB for holes is biased in p-type mode, i. e., $V_{ds} < 0$, and positive V_{gs}-V_T is applied, electrons are injected into the conduction band of the channel by tunneling through the Schottky barrier at drain (red dotted line in Fig. 6.3). The resulting n-branch current exhibits a large inverse subthreshold slope S_1. Reducing V_{gs}-V_T to values in the subthreshold regime suppresses the injection of electrons from drain and enables the injection of holes from source by thermionic emission like in conventional MOSFETs. Therefore, the inverse subthreshold slope S_2 in this regime is close to the thermal limit of 60 mV/dec (green dashed line in Fig. 6.3). A further decrease of V_{gs}-V_T yields in tunneling injection of holes through the Schottky barrier at source when the valence band of the channel is pushed above the Schottky barrier height. In that case, the inverse subthreshold slope S_3 increases since the carrier injection is again determined by a change of the tunneling probability through the Schottky barrier with changing V_{gs} (blue solid line in Fig. 6.3).

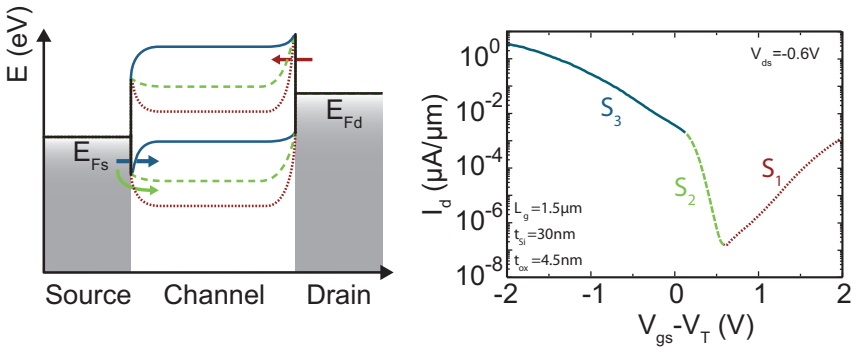

Figure 6.3: Energy band diagrams of an SB-MOSFET in p-type operation (V_{ds} <0) for different gate-source voltages V_{gs} and corresponding transfer characteristic showing the ambipolar switching behavior.

6.3 Long-Channel MOSFETs

The SB-MOSFETs with and without dopant segregation are electrically characterized with a setup composed of a semi-automatic probe system (SÜSS PA 300) and a semiconductor parameter analyzer (HP 4155B). The statistical analysis of 230 to 250 devices of each kind of transistor takes into account any device fluctuations, e.g. substantial variations of the overlap between the gate stack and the silicide contact [18] as well as inhomogeneities of the oxide and silicon thickness [19]. Fig. 6.4 presents a TEM image of long-channel SB-MOSFET with the encroachment of NiSi under the spacer.
The most important device parameters of the long-channel SB-MOSFETs are summarized in Table 6.1.

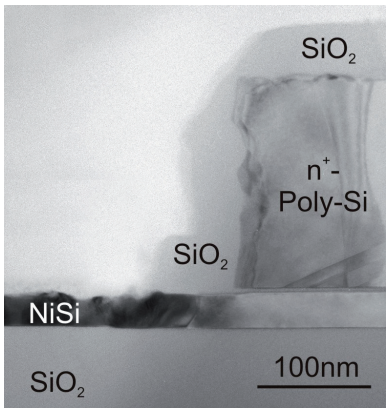

Figure 6.4: TEM image of a long-channel SB-MOSFET showing the encroachment of NiSi under the SiO_2 spacer.

Parameter	**Value**	
t_{Si} (nm)	30	
t_{ox} (nm)	4.5	
L_g (μm)	1.0, 1.5, 2.0, 2.5, 3.0, 3.5, 4.0	
W_g (μm)	10, 20, 30, 40	
Spacer-thickness (nm)	80	
Implantation (at/cm^2)	**As (n-type)**	**B (p-type)**
	$5{\cdot}10^{13}$, $1{\cdot}10^{14}$	w/o
	$5{\cdot}10^{14}$, $1{\cdot}10^{15}$	$5{\cdot}10^{14}$
	$3{\cdot}10^{15}$, $5{\cdot}10^{15}$	$1{\cdot}10^{15}$

Table 6.1: Parameters of n-type and p-type long-channel SB-MOSFETs.

6.3.1 NiSi S/D SB-MOSFETs

Fig. 6.5 shows typical transfer characteristics of a NiSi SB-MOSFETs without dopant segregation, having a gate length of 1.5 μm. The device exhibits the expected ambipolar switching behavior with almost equal on-currents in the n-type branch (V_{gs}-$V_T > 0$) and p-type branch (V_{gs}-$V_T < 0$) for larger V_{ds}. A V_T-shift of approximately -1.1 V is related to the n^+-poly-Si gate stack used for the p-type devices. For the p-type branch, two inverse subthreshold slopes of $S_3 = 77$ mV/dec, close to the thermal limit, and $S_2 = 472$ mV/dec can be extracted, whereas the n-type branch shows only one inverse subthreshold slope of $S_1 = 310$ mV/dec. This is the expected behavior of devices with metallic S/D junctions whose Fermi level is pinned more closely to the valence band than to midgap, which is discussed in Chapter 6.2. In the case of NiSi the Schottky barrier heights are 0.65 eV for electrons and 0.45 eV for holes which is consistent with the observed results [80]. Such high Schottky barriers result in poor on-currents as well as in a poor switching performance since the change of the current in the subthreshold region of SB-MOSFETs is mainly determined by the tunneling probability of carriers through the Schottky barrier which is modulated by the gate-source voltage. Hence, the inverse subthreshold slope is worse than in conventional MOSFETs, where the change in the current flow in the subthreshold regime is determined by the modulation of the potential barrier in the channel. The increase of the n-type branch current with decreasing V_{ds} ($V_{ds2} < V_{ds1} < 0$) is due image-force induced Schottky barrier lowering (cf. Chapter 4.4).

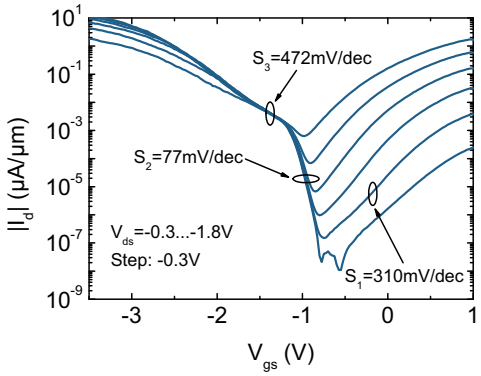

Figure 6.5: Transfer characteristics of SB-MOSFETs with NiSi S/D contacts without dopant segregation. The gate length L_g is 1.5 μm; the SOI and gate oxide thicknesses are $t_{Si} = 30$ nm and $t_{ox} = 4.5$ nm.

Fig. 6.6 shows typical output characteristics (I_d-V_{ds}) of p-type NiSi SB-MOSFETs. At low V_{ds} an exponential onset is apparant instead of a linear current increase which is observed for conventional MOSFETs. This typical property of SB-MOSFETs with a high SBH can be explained by the Schotty barrier-controlled switching where the carriers have to overcome the forward-biased Schottky barrier at drain for low V_{ds}, which vanishes if V_{ds} is increased [13, 81, 82].
Another important finding is, that I_d starts to increase exponentially for high V_{ds}, depending on the applied gate-source voltage which is displayed in Fig. 6.7. This current increase arises due to the ambipolarity of SB-MOSFETs. While the current is dominated by holes flowing from source to drain for small drain-source voltages, a sufficient increase of V_{ds} results in a thinning of the drain Schottky barrier and hence injection of electrons into the conduction band of the channel. Therefore, holes as well as electrons contribute to the current flow.

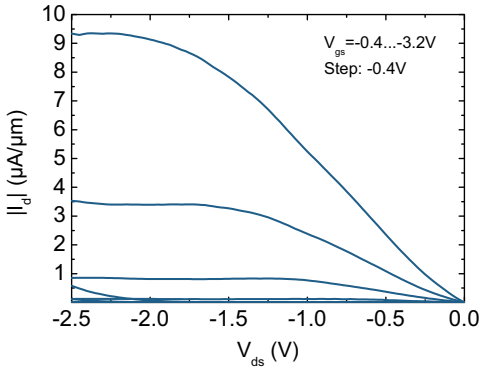

Figure 6.6: Output characteristics of NiSi S/D SB-MOSFET ($L_g = 1.5\,\mu$m).

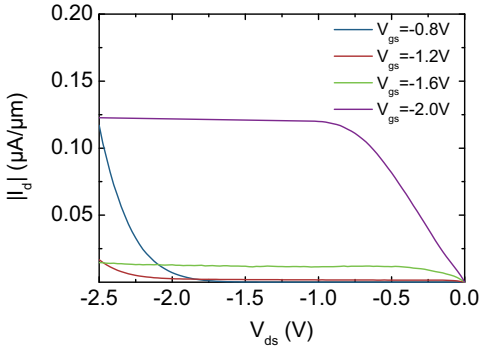

Figure 6.7: Depending on the gate-source voltage, an exponential current inscrease is observed due to the ambipolarity of SB-MOSFETs ($L_g = 1.5\,\mu$m).

6.3.2 p-Type SB-MOSFETs with Dopant Segregation

Transfer characteristics of p-type SB-MOSFETs with boron segregation using a dose of $1{\cdot}10^{15}\,\mathrm{B/cm^2}$ are presented in Fig. 6.8(a). The device shows a strongly improved switching behavior if compared to the NiSi SB-MOSFET presented in Chapter 6.3.1, i. e., we observe only one steep inverse subthreshold slope of 73 mV/dec instead of two slopes. Although, the ambipolar switching behavior is still observed, the n-type branch current is suppressed by two orders of magnitude for the chosen implantation dose. Fig. 6.9 shows schematically the band diagrams of a p-type SB-MOSFET with dopant segregation. The highly B doped segregation layer at S/D of these devices leads to a strong upward band bending at the metal/channel interfaces. Thus, the Schottky barrier for holes is becoming very thin and the tunneling probability through the effectively lowered Schottky barrier gets close to unity. In this case, the modified effective Schottky barrier hardly changes with the gate voltage and the current flow is determined by the potential barrier in the channel as in conventional MOSFETs. At the same time, the injection of electrons from drain is strongly suppressed due to the upward band bending. Fig. 6.8 (b) shows the corresponding output characteristics of a p-type SB-MOSFET which reveal a perfectly linear onset at small V_{ds}.

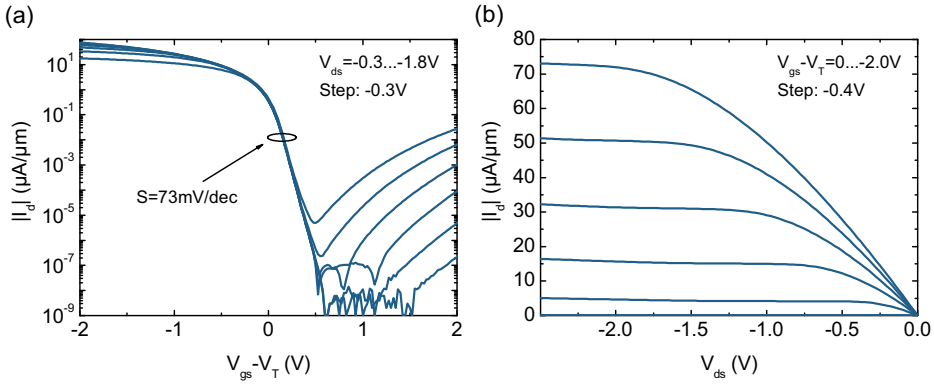

Figure 6.8: (a) Transfer and (b) output characteristics of a p-type SB-MOSFET with dopant segregation using a boron dose of $1{\cdot}10^{15}\,\mathrm{B/cm^2}$ ($L_g = 1.5\,\mu$m).

Fig. 6.10 compares transfer characteristics of p-type SB-MOSFETs with and without dopant segregation using two B^+ implantation doses of $5{\cdot}10^{14}\,\mathrm{B/cm^2}$ and $1{\cdot}10^{15}\,\mathrm{B/cm^2}$. A threshold-voltage correction, as described in Chapter 2.4, is applied to ensure a direct comparision of all devices which might have small variations in V_T. Both SB-MOSFETs with dopant segregation show an improved switching performance when compared to

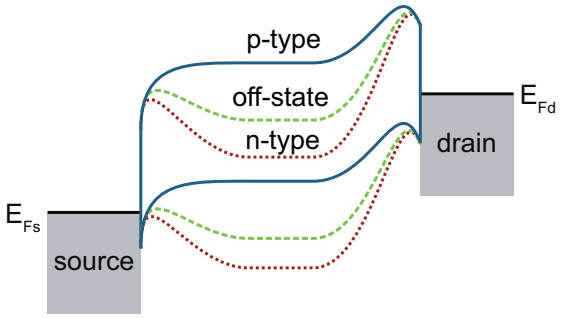

Figure 6.9: Band diagrams of a p-type SB-MOSFET with B segregation at different V_{gs}.

the NiSi SB-MOSFET without dopant segregation. However, the SB-MOSFET with the lower implantation dose still exhibits an n-type branch current similar to the SB-MOSFET without dopant segregation, which could be due to a slight difference in the encroachment of NiSi under the spacer for the two devices. Such variations in the offset between the NiSi and the gate edge result in different electrostatic control over the Schottky barrier by the gate potential. Thus, the resulting variability can easily be observed at low current levels like in the n-type branch of the p-type SB-MOSFETs. An increase of the dopant concentration from $5{\cdot}10^{14}\,\mathrm{B/cm^2}$ to $1{\cdot}10^{15}\,\mathrm{B/cm^2}$ results in an even more reduced effective barrier height for holes while the Schottky barrier for electrons increases. Therefore, the n-type branch current is more suppressed for the higher implantation dose.

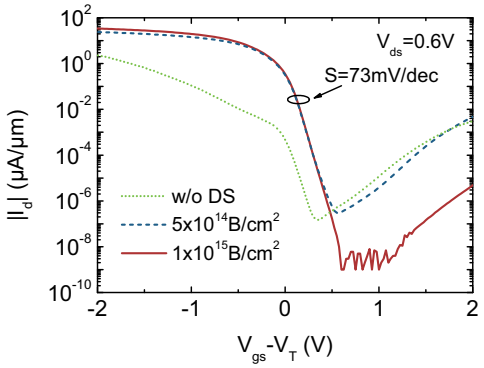

Figure 6.10: Transfer characteristics of p-type SB-MOSFETs with NiSi S/D contacts ($L_g = 1.5\,\mu\mathrm{m}$) with and without B segregation using two implantation doses of $5{\cdot}10^{14}\,\mathrm{B/cm^2}$ and $1{\cdot}10^{15}\,\mathrm{B/cm^2}$.

Fig. 6.11 shows output characteristics of the SB-MOSFETs at V_{gs}-V_T = -1.6 V. It is evident, that the shape of the curves changes substantially for devices with dopant segregation. While an exponential onset, typical of devices with a forward-biased Schottky barrier at drain [13, 81, 82], and a low on-current of around 3.5 μA/μm are observed for devices without dopant segregation, a perfectly linear onset is obtained for SB-MOSFETs with B segregation with high on-currents of 40 μA/μm and 50 μA/μm, respectively.

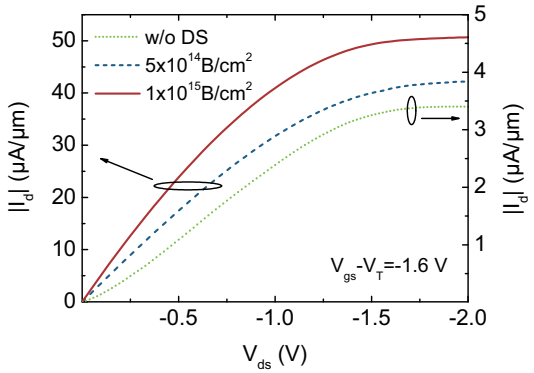

Figure 6.11: Output characteristics of p-type SB-MOSFETs with and without dopant segregation (L_g = 1.5 μm). SB-MOSFETs with boron segregation show a linear onset at small V_{ds}, comparable to conventional MOSFETs. The SB-MOSFET without ion implantation exhibits an exponential onset which is typical of devices with a forward-biased Schottky barrier at drain (cf. Chapter 6.3.1).

The change of the on-currents I_{on} with increasing implantation dose is presented in Fig. 6.12 where averaged on-currents, from statistical measurements, are plotted versus the gate length L_g. SB-MOSFETs with dopant segregation show on-currents, which are one order of magnitude higher than for the pure NiSi SB-MOSFET. Moreover, I_{on} of this SB-MOSFET without dopant segregation does not depend on the gate length within the error bars compared to the other SB-MOSFETs, e.g. doubling the gate length from L_g = 2.0 μm to 4.0 μm results in no change in I_{on} for SB-MOSFETs without dopant segregation whereas a factor of 1.8 is obtained for the other devices. A Schottky barrier, which is still high enough to provide the main contribution to the total resistance R_{tot} can explain this behavior for the NiSi SB-MOSFET. The increasing I_{on} with increasing implantation dose reflects the trend that is already shown in Fig. 6.11.

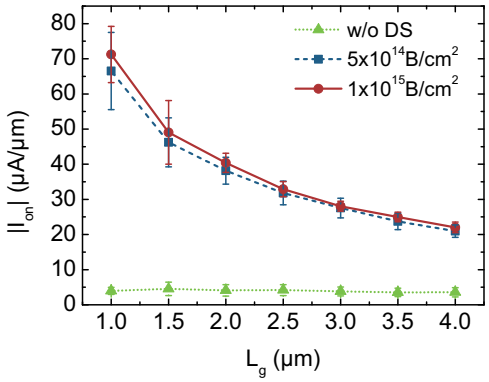

Figure 6.12: Averaged on-currents I_{on} of p-type SB-MOSFETs with different gate lengths from $L_g = 1.5\,\mu$m to $4.0\,\mu$m with and without dopant segregation at V_{gs}-V_T = -1.8 V and V_{ds} = -1.8 V.

6.3.3 n-Type SB-MOSFETs with Dopant Segregation

In case of n-type SB-MOSFETs with dopant segregation a wide range of As^+ implantation doses from $5{\cdot}10^{13}$ As/cm^2 to $6{\cdot}10^{15}$ As/cm^2 is chosen to study the impact of the amount of implanted dopants on the electrical performance of the devices in more detail. Fig. 6.13 shows typical transfer characteristics of n-type SB-MOSFETs with a gate length of $1.5\,\mu$m and different As concentrations at $V_{ds} = 0.6$ V. In the case of As segregation, a strong downward band bending induced by the highly doped As segregation layer changes the electrical characteristics from p-type to n-type by lowering the effective Schottky barrier height for electrons [83]. Therefore, we observe an ambipolar switching with a significantly suppressed p-type branch and an enhanced n-type current for SB-MOSFETs with As segregation. Moreover, we notice a drastic decrease of the p-type branch current with increasing As dopant concentration. Although a slight improvement of the inverse subthreshold slope is visible in Fig. 6.13, the statistical analysis does not reveal such a change. The subthreshold slopes of all devices are close to $S = 100$ mV/dec. Fig. 6.14 shows the corresponding output characteristics at V_{gs}-$V_T = 2$ V. While an exponential onset for small V_{ds} and a low on-current of around $100\,\mu$A/μm at V_{gs}-$V_T = 2$ V and $V_{ds} = 1.8$ V are observed for the device with the lowest implantation dose of $5{\cdot}10^{13}$ As/cm^2, a linear onset for devices with higher implantation doses is measured, indicating a more reduced effective Schottky barrier height. The change in the on-current I_{on} with increasing dose becomes more clear, when Fig. 6.15 is considered where averaged on-currents are plotted versus the As^+ dose for devices with different gate lengths. The largest change in I_{on} is achieved by increasing the

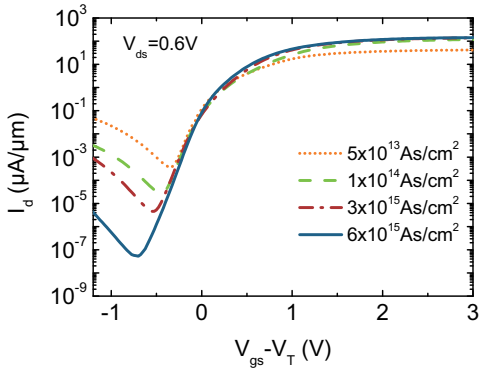

Figure 6.13: Transfer characteristics of n-type SB-MOSFETs using different As^+ implantation doses from $5{\cdot}10^{13}\,As/cm^2$ to $6{\cdot}10^{15}\,As/cm^2$ ($L_g = 1.5\,\mu m$). The improvement of the device performance with increasing implantation doses can easily be seen by more suppressed p-type branches and higher on-currents.

implantation dose from $5{\cdot}10^{13}\,As/cm^2$ to $1{\cdot}10^{14}\,As/cm^2$, which agrees very well with studies of the effective Schottky barrier height on diode structures (cf. Chapter 4.9). Concerning the performance of the devices, the optimum dose seems to be the maximum implantation dose. However, at the highest chosen ion dose of $6 \cdot 10^{15} As/cm^2$ the process yield is only 55%, whereas it is around 89% to 97% for all other samples. In this case, we observe an anomalous high gate leakage current for the non-working devices, which could be due to surface damage of the gate oxide at the gate edge evoked by the high As^+ implantation dose.

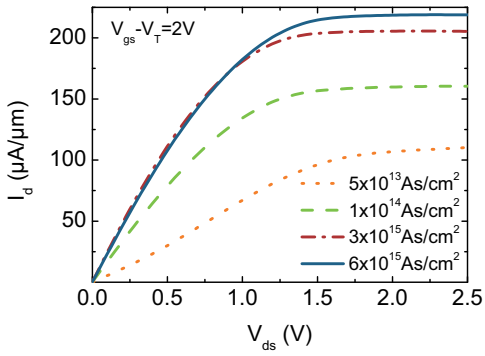

Figure 6.14: Output characteristics of n-type SB-MOSFETs using different As^+ doses from $5{\cdot}10^{13}\,As/cm^2$ to $6{\cdot}10^{15}\,As/cm^2$ ($L_g = 1.5\,\mu m$). For a direct comparison of the curves, a constant value of V_{gs} - V_T is used.

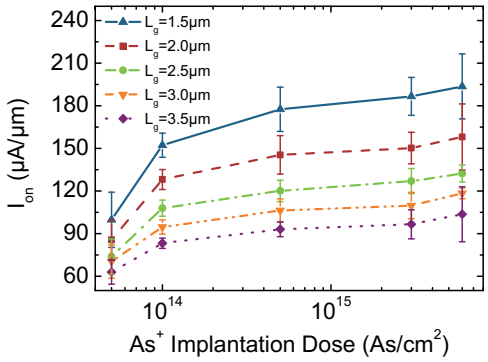

Figure 6.15: On-currents I_{on} of SB-MOSFETs with different implantation doses and channel lengths at V_{gs}-$V_T = 2\,\mathrm{V}$ and $V_{ds} = 1.8\,\mathrm{V}$.

6.3.4 S/D Resistances

When current is flowing from S/D to the channel, four major resistive components contribute to the S/D resistance $R_{s/d}$ in MOSFETs which are visualized schematically in Fig. 6.16. The spreading resistance R_{sp} and accumulation resistances R_{ac} involve a complex analysis of preferential current flow paths when carriers enter the junction. Both components are coupled and depend on the doping gradient and the gate-source voltage. The junction sheet resistance R_{sh} is associated with the conductivity of the highly doped S/D regions or the silicide layers in SB-MOSFETs. Finally, the contact resistance R_{co} is the most significant contribution to the total series resistance [58, 84, 85]. It can be calculated as

$$R_{co} = \frac{\sqrt{\rho_s \rho_c}}{W_g} \coth\left(L_c \sqrt{\frac{\rho_s}{\rho_c}}\right) \tag{6.1}$$

where ρ_s ($\Omega/\square$) is the sheet resistance of the S/D region, ρ_c ($\Omega\mathrm{cm}^2$) the specific contact resistivity which characterizes transport through the silicide/silicon interface, W_g the device width and L_c the contact length [58]. In case of degenerately doped Si where tunneling dominates thermionic emission, the specific contact resistivity can be approximated by:

$$\rho_c \approx \exp\left(\frac{4\pi\sqrt{\varepsilon_{Si} m_{eff}}}{h} \frac{\Phi_B^0}{\sqrt{N}}\right) \tag{6.2}$$

with ε_{Si} the permittivity of the semiconductor, m_{eff} the effective mass, h Planck's constant, Φ_B^0 the Schottky barrier height and N the doping concentration at the silicide/silicon interface. Equation 6.2 highlights the exponential dependence of ρ_c on the Schottky barrier height and the doping level.

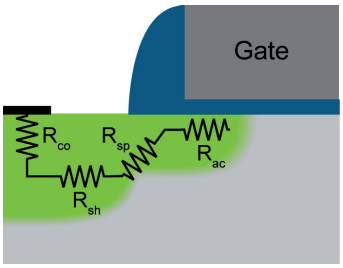

Figure 6.16: Schematic illustration of the S/D resistance which consists of four contributions: contact resistance R_{co}, sheet resistance R_{sh}, spreading resistance R_{sp} and accumulation resistance R_{ac}.

To study the impact of silicidation induced dopant segregation on the S/D resistance the method from Terada *et al.* [86, 87] is applied for the fabricated SB-MOSFETs. The total resistance $R_{tot} = dV_{ds}/dI_d$ is given by

$$R_{tot} = R_{Ch} + R'_{s/d} = \frac{L_g - \Delta L}{W_g \mu_{eff} C_{ox}(V_{gs} - V_T)} + R'_{s/d} \tag{6.3}$$

where R_{Ch} is the channel resistance, W_g the gate width, μ_{eff} the effective mobility and C_{ox} the oxide capacitance. Equation 6.3 provides $R'_{s/d}$ when $L_g = \Delta L$. A plot of R_{tot} versus the gate length L_g for different V_{gs}-V_T is presented in Fig. 6.17. The intersection of the fitted lines yields $R'_{s/d}$ and ΔL. In case of an As dose of $5 \cdot 10^{14}$ As/cm^2 a value of $R_{s/d} = 600\,\Omega\mu$m is extracted, normalized to the gate width of $W_g = 40\,\mu$m, and of ΔL = -0.17 μm. The negative ΔL indicates a channel length which is slightly longer than the designed one, which is in good agreement with a small offset between the NiSi and the edge of the gate stack (compare with Fig. 6.4), but can also be a result of the fabrication process. Fig. 6.18 presents the extracted $R_{s/d}$ values for all implantation doses. As a small drain voltage between V_{ds} = 50-150 mV is used for the extraction of $R_{s/d}$, ensuring device operation in the linear region, the S/D resistance for the lowest implantation dose of $5{\cdot}10^{13}$ As/cm^2 has to be regarded carefully. In this case, SB-MOSFETs still exhibit an exponential onset for small V_{ds} and not the preconditioned linear onset which is present for all other devices with higher implantation doses. A strong decrease of $R_{s/d}$ is found with increasing implantation doses to a minimum value of around 560 $\Omega\mu$m which is in good agreement with results obtained from *S*-parameter measurements (see Chapter 7.5.1). For the p-type SB-MOSFETs with the highest implantation dose of $1{\cdot}10^{15}$ B/cm^2, a S/D resistance of around 1600 $\Omega\mu$m is obtained. Even lower resistances are expected by optimization of the process flow as well as a combination of dopant segregation with elevated S/D.

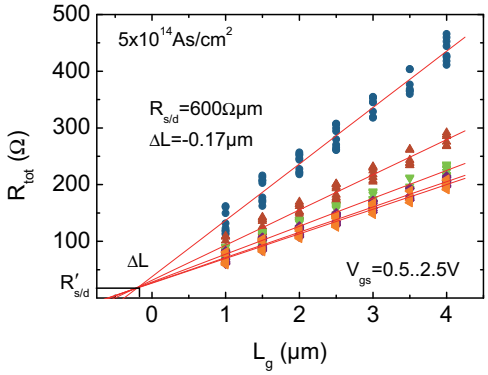

Figure 6.17: Total resistance R_{tot} versus the gate-length L_g as a function of gate-source voltage V_{gs} for SB-MOSFETs with dopant segregation using an implantation dose of $5 \cdot 10^{14}\,\mathrm{As/cm^2}$. The gate width is $W_g = 40\,\mu\mathrm{m}$.

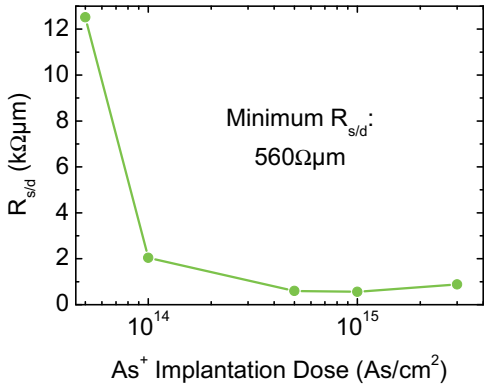

Figure 6.18: Averaged $R_{s/d}$ values versus the As^+ implantation dose. A minimum $R_{s/d}$ of $560\,\Omega\mu\mathrm{m}$ is extracted.

6.4 Short-Channel SB-MOSFETs

Fig. 6.19 presents a cross-sectional TEM image of a short-channel SB-MOSFET with a gate length of 80 nm. The encroachment of NiSi into the channel region is clearly visible, as well as the partially silicided n^+-poly-Si gate stack. The latter offers a great advantage for the RF-performance because of the reduction of the gate resistance which will be presented in Chapter 7.5.1. The most important device parameters of the short-channel SB-MOSFETs are summarized in Table 6.2.

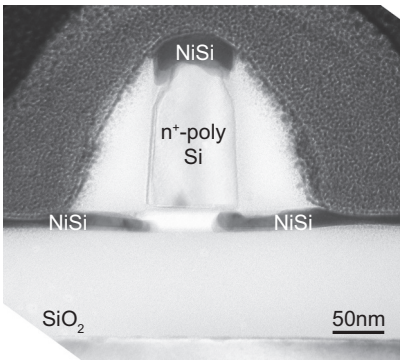

Figure 6.19: Cross-sectional TEM image of a readily fabricated short-channel SB-MOSFET with a 3.5 nm-thick gate oxide and a 160 nm-thick n^+-poly-Si gate, showing the encroachment of NiSi into the channel region.

Parameter	**Value**	
t_{Si} (nm)	20	
t_{ox} (nm)	3.5	
L_g (nm)	80, 180, 280, 380	
W_g (μm)	$2 \cdot 40$, $2 \cdot 100$	
Spacer-thickness (nm)	75	
Implantation (at/cm^2)	**As (n-type)**	**B (p-type)**
	$3{\cdot}10^{15}$	$3{\cdot}10^{15}$

Table 6.2: Parameters of n- and p-type short-channel SB-MOSFETs.

Typical transfer and output characteristics of p-type SB-MOSFETs with a gate length of 80 nm are presented in Fig. 6.20. The device exhibits an inverse subthreshold slope of $S = 106\,\mathrm{mV/dec}$. In contrast to long-channel SB-MOSFETs, these devices suffer from short-channel effects (cf. Chapter 2.5). Drain induced barrier lowering with a value of 208 mV/V is pronounced by a threshold-voltage shift in the transfer characteristics with increasing V_{ds}. In the output characteristics, DIBL results in a finite slope in saturation of the SB-MOSFET instead of a constant saturation current as for long-channel devices. The exponential onset in the output characteristics at small V_{ds}, Fig. 6.20(b), is a typical property of SB-MOSFETs with a relatively high Schottky barrier height as already discussed in Chapter 6.3.1. The larger Schottky barrier height is a consequence of a poor selectivity between SiO_2 and Si during spacer etching, which resulted in an overetch of the highly implanted S/D regions and consequently in a loss of the shallow implanted B atoms. As a result of the high parasitic S/D resistance, the current

saturates only at high V_{ds} and even at V_{ds} = -1.8 V the maximum transconductance $G_{m,DC}$ is not reached (cf. Fig. 6.21).

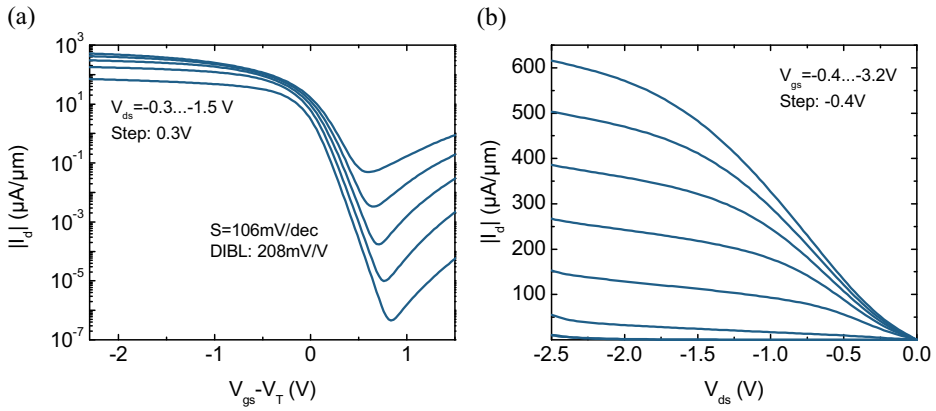

Figure 6.20: (a) Transfer and (b) output characteristics of p-type SB-MOSFETs with dopant segregation using an implantation dose of $3{\cdot}10^{15}$ B/cm^2 (L_g = 80 nm).

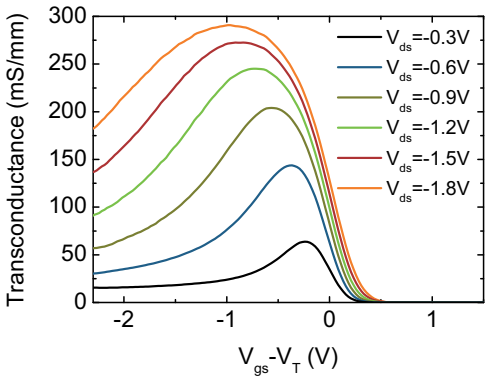

Figure 6.21: Transconductance of a 80 nm-short channel p-type SB-MOSFET with dopant segregation using an implantation dose of $3{\cdot}10^{15}$ B/cm^2.

Fig. 6.22(a) shows transfer characteristics of p-type SB-MOSFETs with different gate lengths of L_g =80 nm to 380 nm at V_{ds} = 0.3 V. The inverse subthreshold slope is about 75 mV/dec for all devices except for the 80 nm-short channel where S is 106 mV/dec. While DIBL shows only a value of 20 mV/V for gate-lengths down to 180 nm, the 80 nm-short channel SB-MOSFET shows a value of 208 mV/V as shown in Fig. 6.20. The V_T-roll-off ΔV_T is found to be 0.5 V in average at V_{ds} =- 0.3 V for devices with L_g =80 nm in comparison to the long-channel case (see Fig. 6.23). The larger ΔV_T-values at V_{ds} =- 0.9 V in comparison to ΔV_T at V_{ds} =- 0.3 V are result of the drain induced barrier

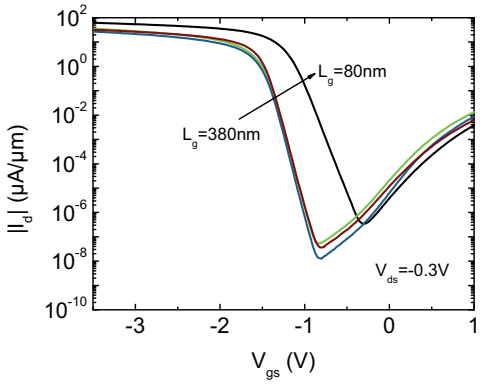

Figure 6.22: Transfer characteristics of p-type SB-MOSFETs with different gate lengths of L_g =80 nm to 380 nm at V_{ds} = -0.3 V. The shortest channel length shows a strong V_T-roll-off.

lowering (DIBL) when the drain-source voltage is changed. The increase of the on-current I_{on} with decreasing gate length from 380 nm to 80 nm is presented in Fig. 6.24 at V_{gs}-V_T = -2.0 V and V_{ds} = -1.2 V/-1.5 V.

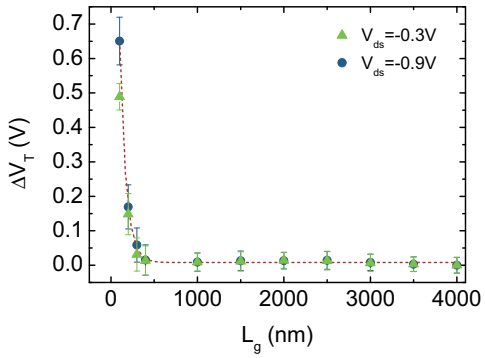

Figure 6.23: V_T-roll-off ΔV_T of p-type SB-MOSFETs with dopant segregation plotted as a function of the gate length at V_{ds} = -0.3 V and V_{ds} = -0.9 V.

Fig. 6.25 shows typical transfer and output characteristics of n-type SB-MOSFETs with a gate length of 80 nm. Since these devices show threshold voltages close to 0 V, no V_T correction is applied here. DIBL with a value of 290 mV/V is slightly larger than for the 80 nm-short channel p-type SB-MOSFET presented before. The inverse subthreshold slope S is degraded from 100 mV/dec in case of the long-channel n-type SB-MOSFETs to 128 mV/dec for the 80 nm devices. An averaged on-current I_{on} of 960 μA/μm at V_{gs} = 2.5 V and V_{ds} = 1.2 V is obtained for devices with the shortest channel length.

Fig. 6.26 shows the increase of I_{on} with decreasing gate length from $L_g = 380\,\text{nm}$ to 80 nm for $V_{gs} = 2.5\,\text{V}$ and $V_{ds} = 1.2\,\text{V}$.

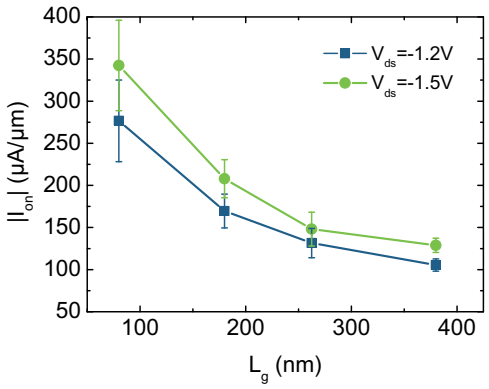

Figure 6.24: Increase of I_{on} of p-type SB-MOSFETs ($3{\cdot}10^5\,\text{B/cm}^2$) with decreasing gate length at V_{gs}-V_T =- 2.0 V and V_{ds} =- 1.2 V/-1.5 V.

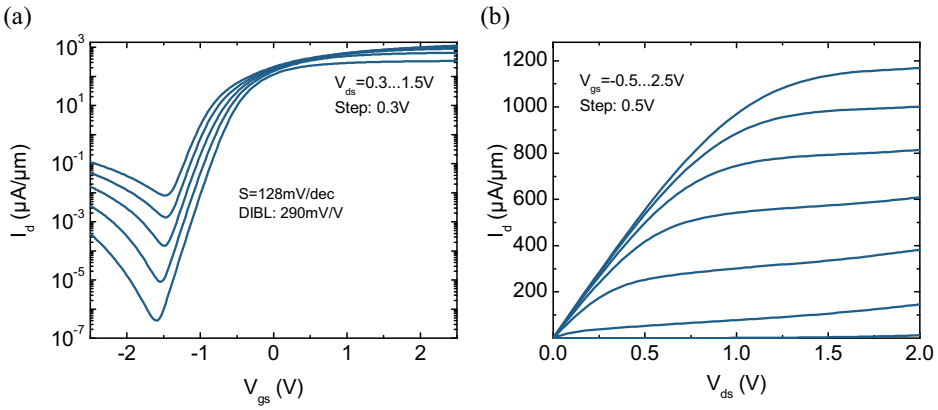

Figure 6.25: (a) Transfer and (b) output characteristics of an n-type SB-MOSFET with NiSi S/D contacts ($L_g = 80\,\text{nm}$).

The DC transconductance of the 80 nm-short channel SB-MOSFET is presented in Fig. 6.27. The maximum transconductance $G_{m,DC}$ of 450 μS/μm is achieved at $V_{gs} \approx 0.4\,\text{V}$ and V_{ds} between 0.9 and 1.2 V. The decrease of the transconductance with higher gate-source voltages is related to the mobility degradation for high electric fields [24], since $G_m \propto \mu_{eff} C_{ox}(V_{gs} - V_T)$ (cf. Chapter 2.4).

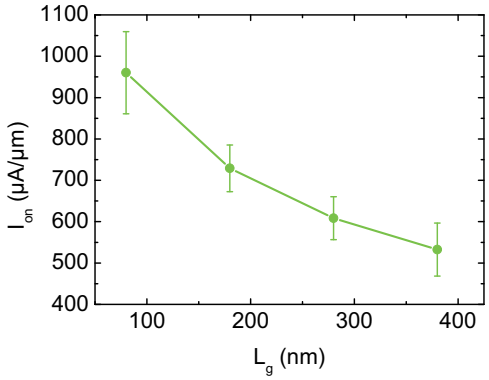

Figure 6.26: Increase of I_{on} of n-type SB-MOSFETs with decreasing gate length at $V_{gs} = 2.5\,\mathrm{V}$ and $V_{ds} = 1.2\,\mathrm{V}$.

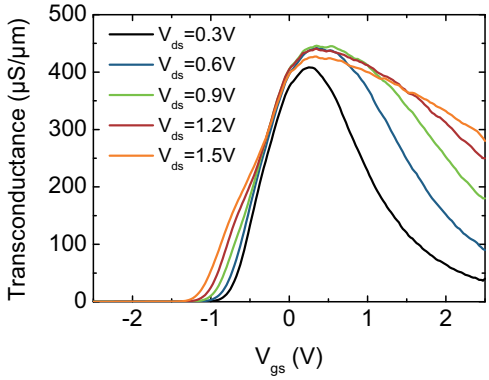

Figure 6.27: Transconductance of an 80 nm-short channel n-type SB-MOSFET with dopant segregation using an implantation dose of $3{\cdot}10^{15}\,\mathrm{As/cm^2}$.

6.5 Optimized Devices

The device parameters of n-type SB-MOSFETs fabricated with the optimized spacer etching process are summarized in Table 6.3. The main differences to the devices presented in Chapter 6.4 are thinner SiO_2 gate-spacers ($\approx$10 nm) which simplify the control of the NiSi encroachment under the spacer. Moreover the optimized process avoids a loss of the highly implanted Si at the S/D regions during spacer etching.

Parameter	Value
t_{Si} (nm)	20
t_{ox} (nm)	3.5
L_g (nm)	80, 180, 280, 380
W_g (μm)	$2 \cdot 40$, $2 \cdot 100$
Spacer-thickness (nm)	$\approx$10
Implantation (at/cm^2)	**As (n-type)**
	$5{\cdot}10^{13}$, $1{\cdot}10^{14}$, $5{\cdot}10^{14}$ $1{\cdot}10^{15}$, $3{\cdot}10^{15}$, $3{\cdot}10^{15}$

Table 6.3: Parameters of optimized n-type short-channel SB-MOSFETs.

Fig. 6.28 shows transfer and output characteristics of n-type short-channel SB-MOSFETs ($L_g = 180$ nm) with dopant segregation using different As doses. In contrast to the long-channel devices, presented in Chapter 6.3.3, the SB-MOSFET with the lowest dose of $5 \cdot 10^{13}$ As/cm^2 exhibits almost equal on-currents for the p- and n-branches, indicating that the effective Schottky barrier height for electrons is still close to the original value, whereas a significantly reduced p-branch is apparent for devices with higher dose. Moreover, the output characteristics reveals an exponential onset at low V_{ds} even at a dose of $1 \cdot 10^{14}$ As/cm^2. This unexpected behavior can be related to the different spacer thickness for the long-channel and the short-channel SB-MOSFETs. The shorter lateral segregation length during silicidation through the highly doped Si in case of the 180 nm-short channel SB-MOSFETs results in a smaller pile-up of

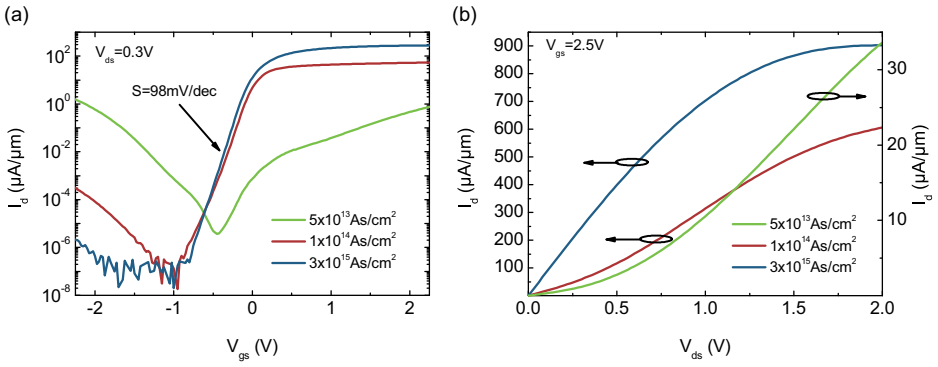

Figure 6.28: (a) Transfer and (b) output characteristics of SB-MOSFETs with dopant segregation using different As doses from $5{\cdot}10^{13}$ As/cm^2 to $3{\cdot}10^{15}$ As/cm^2 ($L_g = 180$ nm). The improvement of the device performance with increasing As dose can easily be seen by much lower p-branches and higher on-currents.

dopants at the NiSi/Si interface if compared to the longer segregation length in case of a thicker spacer. As a result, the modulation of the barrier height is less efficient, although the same implantation dose is used. The RF performance of these devices with different Schottky barrier heights is presented in Chapter 7.7.2. Fig. 6.29(a) shows the transfer characteristics of an optimized 80 nm-short channel device with an As dose of $3 \cdot 10^{15}$ As/cm^2. The inverse subthreshold slope S is 118 mV/dec; DIBL amounts to 370 mV/V. The result of the process optimization is clearly visible in Fig. 6.29(b), where the optimized (blue solid line) and the SB-MOSFET, presented in Chapter 6.4 (green solid line), are compared. A minimization of the unintentional Si-etching results in lower S/D resistances and therefore an earlier current saturation at lower V_{ds}. The extraction of the extrinsic resistances in Chapter 7.7.1 quantifies this qualitative finding. Please note, that a small V_T-shift of approximately 200 mV between these two devices forbids a direct comparison of the on-currents.

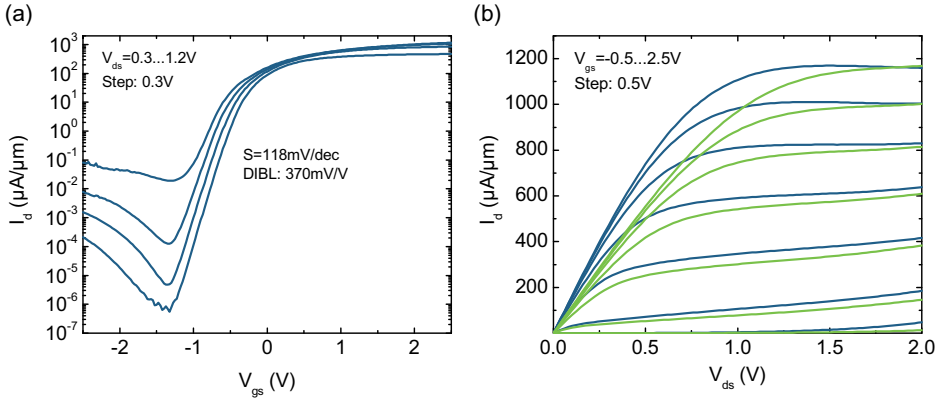

Figure 6.29: (a) Transfer characteristics of an 80 nm-short channel SB-MOSFET ($3{\cdot}10^{15}$ As/cm^2). (b) Comparison of the output characteristics of an optimized (blue solid line) SB-MOSFET and a device with the same gate-length (Chapter 6.4) using an unoptimized process flow (green solid line).

6.6 Strained SOI

The use of high mobility channel materials strongly improves the electrical performance of ultimately scaled CMOS devices. Therefore, tensile or compressive strained Si channels for high electron or hole mobilities are integrated in leading edge fabrication processes for high performance applications [88]. Besides process-induced local stress

by stress liners or stress memorization techniques [89], global biaxial strain in the lattice structure of crystalline silicon is obtained by epitaxial growth of thin Si layers on top of relaxed SiGe substrates [90, 91]. As a result of strain, the six-fold degenerated valleys of Si are split into two sets, the in-plane $\Delta 4$-valleys and the energetically lower out-of-plane $\Delta 2$-valleys, whose energy splitting strongly depends on the stress level [92, 93]. Recently, it has been experimentally shown, that the mobility enhancement observed in MOSFETs fabricated on biaxially tensile strained SOI (sSOI) is caused by the occupation of the $\Delta 2$-valleys with low electron effective mass in transport direction and by reduced intervalley phonon scattering due to a lower k-space volume and not by a reduction of the effective mass [94].
Therefore, it is attractive to combine the Schottky barrier concept with high-mobility Si. These devices are fabricated on 25 nm-thick biaxially tensile strained SOI with the optimized process flow using implantation doses of $3{\cdot}10^{15}$As/cm^2 for n-type and $3{\cdot}10^{15}$B/cm^2 for p-type SB-MOSFETs. Besides the one-step annealing which is used for all devices presented before, a two-step annealing is used. This consists of an annealing at 280°C for 10 min where nickel-rich silicide is formed, followed by selective etching of the unreacted Ni and a second annealing at 450°C for 30 sec where nickel-monosilicide is formed. The two-step annealing simplifies the control of NiSi encroachment under the spacer when extremely thin spacers are used. Fig. 6.30 shows a cross-sectional TEM image of an 80 nm-short channel SB-MOSFET fabricated on 25 nm thick sSOI with its NiSi S/D regions.

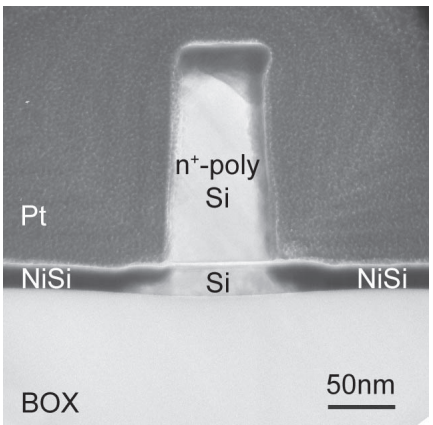

Figure 6.30: Cross-sectional TEM image of a SB-MOSFET fabricated on 25 nm-thick sSOI with a buried oxide thickness of 140 nm.

The transfer and output characteristics of 180 nm-short channel p-type devices on SOI and sSOI are presented in Fig. 6.31. As expected, the performance of the strained p-type SB-MOSFETs is comparable to the one of the SOI devices. Slight variations of the inverse subthreshold slope and the off-state current in the transfer characteristics and of the exponential onset in the output characteristics might be results of process fluctuations.

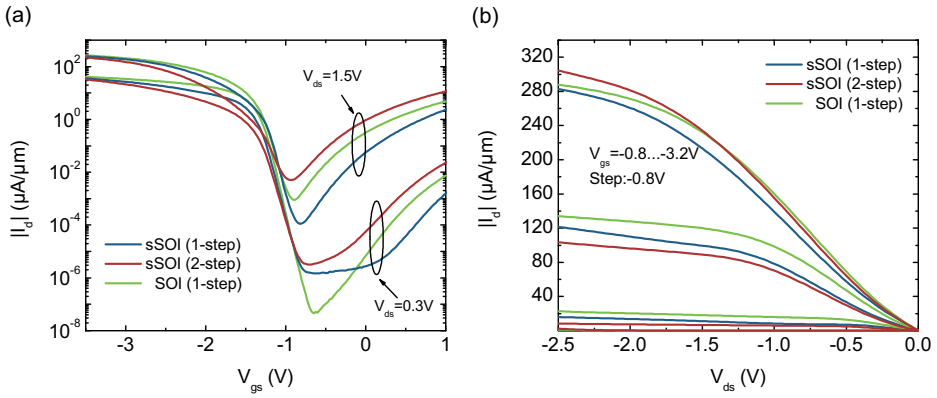

Figure 6.31: (a) Transfer and (b) output characteristics of a 180 nm-short channel p-type SB-MOSFETs fabricated on sSOI and SOI.

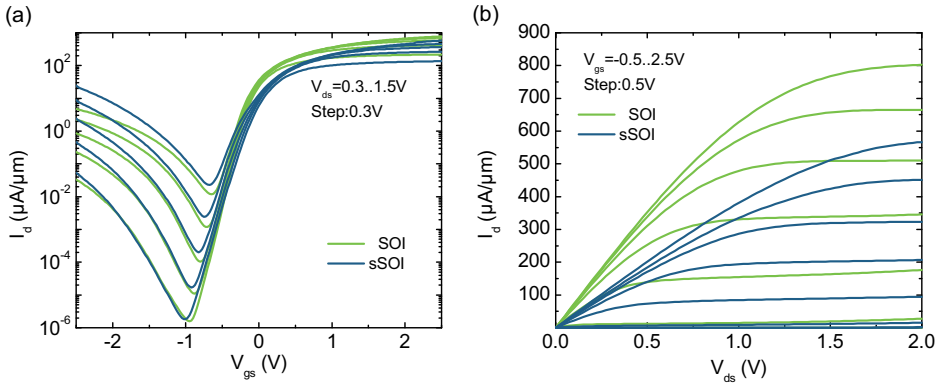

Figure 6.32: (a) Transfer and (b) output characteristics of a 180 nm-short channel n-type SB-MOSFETs fabricated on sSOI and SOI.

In case of n-type SB-MOSFETs fabricated using a one-step annealing an improvement of the device performance is assumed for strained Si devices due to the electron mobility

enhancement. However, the electrical characteristics which are shown in Fig. 6.32 are inferior to the SB-MOSFETs fabricated on SOI, i. e., lower on-currents and a less steep linear onset, indicating higher S/D resistances, are observed. This unexpected behavior might be related to a poor lateral segregation of As through the strained Si or contact problems due to an abnormal oxidation of NiSi in the vicinity of highly As-doped Si [95]. Such an oxide layer on top the NiSi is clearly visible in Fig. 6.30 as a bright layer between the NiSi and the Pt. This interlayer increases the contact resistance of the Cr/Al metallization on NiSi.

6.7 Benchmarking

A comparison with the state-of-the-art SB-MOSFETs in Fig. 6.33 and Fig. 6.34 demonstrates the superior performance of the NiSi SB-MOSFETs presented in this work. The black squares in both figures indicate various results of MOSFETs with pure Schottky contacts without DS [12].
The p-type SB-MOSFETs exhibit an on-current I_{on} of 427 μA/μm at V_{gs}-V_T = -2.8 V and V_{ds} = -1.2 V with an I_{on}/I_{off}-ratio of 10^4. At V_{ds} = -1.5 V even higher values of I_{on} = 525 μA/μm are obtained. Therefore, the performance of the p-type SB-MOSFETs is similar to p-type devices fabricated by IEMN with dopant segregation using PtSi [17]. A better performance is only achieved with devices which are fabricated on process-strained bulk SiGe by TSMC [96].
In the case of n-type SB-MOSFETs only devices with NiSi S/D show high on-currents whereas rare earth silicides still show poor I_{on}/I_{off} ratios. The SB-MOSFETs of this work with the optimized process flow show excellent values of I_{on} of 1150 μA/μm at V_{gs} = 2.5 V and V_{ds} = 1.2 V. These values are much better than for devices fabricated on bulk Si by Toshiba [97]. Only devices with process-induced strained-channels fabricated by TSMC [96] show better performance. Please note, that the thick gate oxide of around 3.5 nm yields a conservative value for I_{on} at V_{gs}-V_T = -2.8 V for the p-type devices and V_{gs} = 2.5 V for the n-type SB-MOSFETs. The effective fields at these bias conditions are lower than for $|V_{gs}|$ = 1.1 V, the standard value for benchmarking with a 1.2 nm thick gate-oxide.

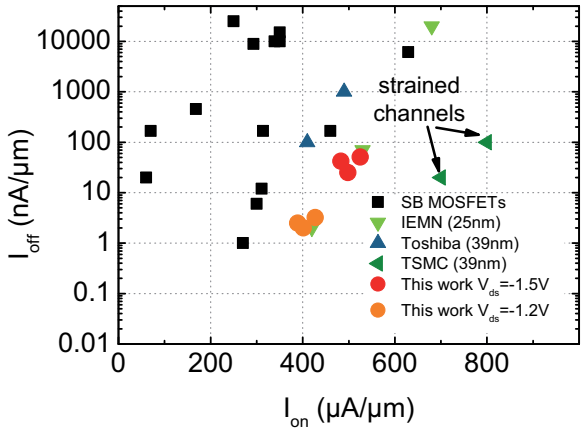

Figure 6.33: I_{on}-I_{off} state-of-the-art of p-type SB-MOSFETs [12, 17, 96, 97]. The p-type SB-MOSFETs of this work have an oxide thickness of $t_{ox} = 3.5\,\text{nm}$ and are measured at V_{gs}-V_T = -2.8 V. The values given in brackets refer to the gate lengths of the SB-MOSFETs.

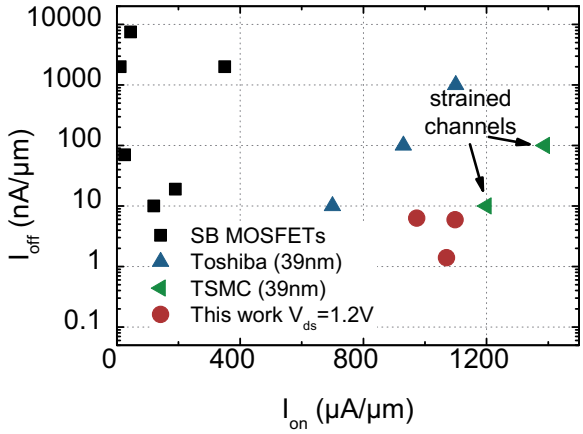

Figure 6.34: I_{on}-I_{off} state-of-the-art of n-type SB-MOSFETs [12, 96, 97]. The n-type SB-MOSFETs of this work exhibit an oxide thickness of $t_{ox} = 3.5\,\text{nm}$ and are measured at $V_{gs} = 2.5\,\text{V}$. The values given in brackets refer to the gate length of the SB-MOSFETs.

6.8 Summary

A detailed study of long-channel as well as short-channel p- and n-type SB-MOSFETs is presented. Devices with silicidation induced dopant segregation show drastically improved DC performance when compared to SB-MOSFETs without ion implantation. Thus, SB-MOSFETs with B segregation show an improved on-current by one order of magnitude if compared to devices with pure NiSi S/D contacts. Studies of the dopant dependence on the device performance show that the correct choice of the implantation dose in combination with the spacer thickness, i. e., the segregation length, is mandatory to achieve superior electrical characteristics. Generally, the analysis of the devices shows that increasing the implantation dose results in a better performance of the SB-MOSFETs with higher on-currents and a distinct suppression of the ambipolar behavior. An extraction of the S/D resistances of long-channel n-type SB-MOSFETs reveals a strong reduction for devices with high As dose. A minimum value of $R_{s/d}$ of $560\,\Omega\mu$m is extracted for SB-MOSFETs on 30 nm thick SOI.
The short-channel SB-MOSFETs with $L_g = 80$ nm show high performance comparable to state-of-the-art devices. The on-currents are as high as $427\,\mu$A/μm at V_{gs}-V_T = -2.8 V and V_{ds} = -1.2 V for p-type SB-MOSFETs and $1150\,\mu$A/μm at $V_{gs} = 2.5$ V and $V_{ds} = 1.2$ V for the n-type devices. Even higher values are expected by combination of dopant segregation with elevated source and drain. Moreover, a reduction of the natural length λ would result in a reduction of SCE, i. e., DIBL and V_T-roll-off [98]. This could be achieved by using thinner SOI, high-k gate-dielectrics or even different device architectures like double gate or nanowire SB-MOSFETs, for instance. SB-MOSFETs fabricated on biaxially strained SOI show similar DC performance for p-type devices when compared with SOI devices. However, in case of n-type SB-MOSFETs, where a performance increase is expected due to a higher effective electron mobility, degraded performance is observed which could be a result of a worse segregation of As dopants or a contact problem due to abnormal oxidation of NiSi in the presence of strained silicon.

Chapter 7

RF-Characterization

This chapter provides a detailed radio-frequency (RF) analysis of dopant-segregated n- and p-type SB-MOSFETs. The fundamentals of scattering S parameters and the small-signal equivalent circuit of a MOSFET are introduced, followed by a brief description of the characterization method and the measurement procedure. The extrinsic and intrinsic device parameters are extracted as a function of the device dimensions, i. e., the gate length L_g and the gate width W_g. Finally, for the first time RF performance of n-type SB-MOSFETs with dopant segregation using different implantation doses is investigated. This provides an in-depth understanding of the frequency dependence of SB-MOSFETs having different Schottky barrier heights. A comparison with state-of-the art devices demonstrates the superior performance of the 80 nm-short channel devices.

7.1 Scattering-Parameters

Scattering or S-parameters are used for the characterization of n-port networks and allow an extraction of important figures of merit such as the cut-off frequency f_T and the maximum oscillation frequency f_{max}. Although, various other network analysis methods exist [99, 100], S-parameters hold the advantage that no open and short circuits are required for measurements whereas H-, Y- and Z-parameter sets which relate total voltages and total currents at each of the two ports rely on short and open measurements. This is a crucial point for the RF characterization because of the difficulty to achieve short and open over a broad band of frequencies.
For the characterization of a two-port network the scattering matrix (S) relates the power levels of the incident (a_1, a_2) and reflected waves (b_1, b_2) at the input (1) and

output (2) port of the device linearily :

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{7.1}$$

The S-parameters are determined by performing following measurements:

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \qquad S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \tag{7.2}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \qquad S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} \tag{7.3}$$

The circuitry which is used to determine the input reflection S_{11} and forward transmission coefficient S_{21} (top) and of the output reflection S_{22} and reverse transmission coefficient S_{12} (bottom) of a two-port network is shown in Fig. 7.1. The condition, that $a_1 = 0$ or $a_2 = 0$ means that no power is injected at port 1 or port 2, respectively. Thus, to measure S_{11} and S_{21}, the power source is applied at port 1 ($a_1 \neq 0$) and port 2 is configured in load mode, i. e., $a_2 = 0$ and the load impedance Z_L is equal to $50\,\Omega$. For the measurement of S_{22} and S_{12} the source and load configuration at the two ports is changed.

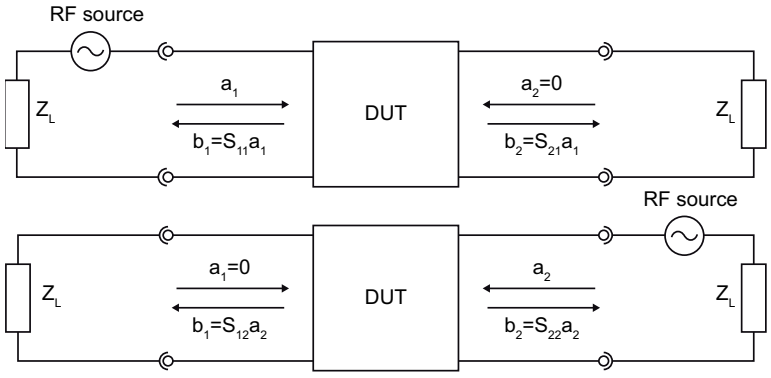

Figure 7.1: Circuitry for the determination of the S-parameters S_{11} and S_{21} (top) and S_{12} and S_{22} (bottom).

7.2 Small-Signal Model of the SOI MOSFET

Before describing the extraction techniques which are used for the characterization of the SB-MOSFETs, the elements of the equivalent circuit are introduced and identified in the physical structure of the MOSFET [101].

7.2.1 Useful Transistor Effect

The current modulation of I_d by the applied V_{gs} can be modeled by a current source between source and drain controlled by a potential applied to the input (gate-to-source capacitance). Fig. 7.2 shows the intrinsic gate transconductance G_{mi} and the intrinsic gate-to-source capacitance C_{gsi} of the SOI MOSFET. The index "i" denotes the intrinsic elements which model the useful transistor effect and which are thus dependent on the bias conditions and on the device dimensions or more precisely on the size of the active zone [102]. Although, the equivalent circuit presented in Fig. 7.2 models the characteristics of a MOSFET, the parasitic elements which are present in real devices have to be introduced in the following to obtain a complete small-signal equivalent circuit of the SOI MOSFET.

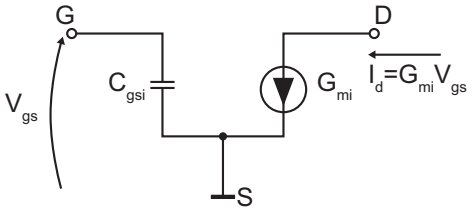

Figure 7.2: Equivalent circuit of the useful MOSFET effect [102].

7.2.2 Quasi-Static Model

In the quasi-static model proposed by Tsividis which is based on the quasi-static charge sheet model, the capacitance effects of every contact on every other are modeled [103]. The capacitances are defined for small-signal voltages which vary sufficiently slowly such that nonquasi-static effects which are linked to the distribution of charges in the channel can be neglected. Therefore, the slopes of the form $\partial q_k/\partial v_l$, where q_k is any of the four charges (source, drain, gate, substrate) and v_l any of the voltages are assumed constant and equal to their value at the DC bias point, denoted by "o":

$$C_{kki} = \left.\frac{\partial q_k}{\partial v_k}\right|_o \tag{7.4}$$

$$C_{kli} = \left.\frac{\partial q_k}{\partial v_l}\right|_o \qquad l \neq k \tag{7.5}$$

In general $C_{kli} \neq C_{lki}$ which can be easily unterstood by considering a long-channel MOSFET in saturation, where a change in V_{ds} does not change the device characteristics and hence, C_{gdi} is zero. However, varying V_{gs} changes the inversion layer charge

whose change is accomplished in part by the drain current temporarily becoming different from the transport value. Under small-signal conditions this difference is equal to $-C_{dgi}(dv_g/dt)$, which can only be nonzero if $C_{dgi} \neq 0$.
In case of SOI MOSFETs substrate effects can be neglected as long as the thickness of the BOX is large in comparison to the top gate. Therefore, the SOI MOSFET is modeled only by three terminals as shown in Fig. 7.3. Since MOSFETs are imperfect current sources, an output conductance is introduced in the model which is defined by:

$$G_{dsi} = \left.\frac{\partial i_d}{\partial v_{ds}}\right|_o \tag{7.6}$$

Y_{mi} in Fig. 7.3 represents the gate transadmittance and is defined by:

$$Y_{mi} = G_{mi} - j\omega C_{mi} \tag{7.7}$$

where G_{mi} is the intrinsic transconductance and C_{mi} the transcapacitance which accounts for non-reciprocal effects which appear when developing complete charge models of transistors [102]. It is given by

$$C_{mi} = C_{dgi} - C_{gdi} \tag{7.8}$$

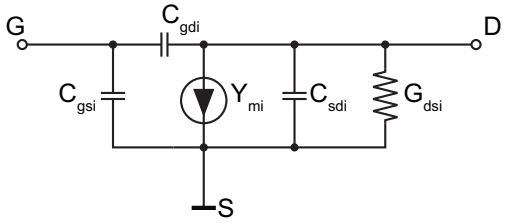

Figure 7.3: Intrinsic quasi-static model [102, 103].

7.2.3 Nonquasi-Static Model

In the nonquasi-static case, where variations of the small-signal voltage v_s are fast, the inversion layer charge becomes non-negligible and the effect of the changing gate charge lags behind the source voltage change. This relaxation phenomenon cannot be modeled by a capacitance between source and gate anymore, but by the intrinsic series resistances R_{gsi} and R_{gdi} in series with the intrinsic capacitances, respectively, C_{gsi} and C_{gdi} [103]. The nonquasi-static model is shown in Fig. 7.4 where τ models the propagation time delay of charges in the channel from source to drain. The corresponding Y-matrix is given by:

$$Y_{\pi i} = \begin{bmatrix} j\omega\left(\frac{C_{gsi}}{D_{gsi}} + \frac{C_{gdi}}{D_{gdi}}\right) & -j\omega\frac{C_{gdi}}{D_{gdi}} \\ \frac{G_{mi}e^{-j\omega\tau}}{D_{gsi}} - j\omega\frac{C_{gdi}}{D_{gdi}} & G_{dsi} + j\omega\left(C_{sdi} + \frac{C_{gdi}}{D_{gdi}}\right) \end{bmatrix} \tag{7.9}$$

with $D_{gsi} = 1 + j\omega R_{gsi}C_{gsi}$ and $D_{gdi} = 1 + j\omega R_{gdi}C_{gdi}$.

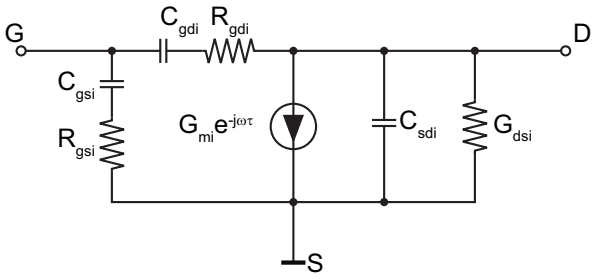

Figure 7.4: Intrinsic nonquasi-static model.

7.2.4 Extrinsic Model and Access Elements

The intrinsic parameters presented in the sections before depend on the bias conditions and the dimensions of the MOSFET. However, the MOSFET includes also some elements which are constant versus bias or even independent of the size of the MOSFET. These parameters are called "extrinsic" and are denoted by an index "e".

Extrinsic Capacitances

The extrinsic gate-to-source C_{gse} and gate-to-drain C_{gde} capacitances are the parallel combinations of fringing effects between the gate-stacks and the S/D regions and of overlap capacitances which are caused by diffusion of dopants or in case of SB-MOSFETs by an enchroachment of silicide under the gate stack. The locations of the extrinsic capacitances in a MOSFET are presented in Fig. 7.13 where C_{dse} models the source-drain proximity capacitance.
The new Y_{π}-matrix is obtained by adding the extrinsic capacitances to the imaginary parts of the $Y_{\pi i}$-matrix elements of Equation 7.9.

Extrinsic Series Resistances

The source, drain and gate fingers constitute the connections between these three external contacts and the intrinsic part of the transistor. The distribution of these resistances is modeled by equivalent lumped resistances R_{Se}, R_{De} and R_{Ge} connected to the source, drain and gate contacts. Similar to this, the inductances are modeled by equivalent lumped inductances L_{Se}, L_{De} and L_{Ge}. The Z-matrix of the equivalent circuit presented in Fig. 7.5 is defined by:

$$Z_{\Sigma\pi} = Z_{\Sigma} + Y_{\pi}^{-1} \tag{7.10}$$

$$\text{with} \quad Z_{\Sigma} = \begin{bmatrix} R_{Ge} + R_{Se} & R_{Se} \\ R_{Se} & R_{De} + R_{Se} \end{bmatrix} + j\omega \begin{bmatrix} L_{Ge} + L_{Se} & L_{Se} \\ L_{Se} & L_{De} + L_{Se} \end{bmatrix} \tag{7.11}$$

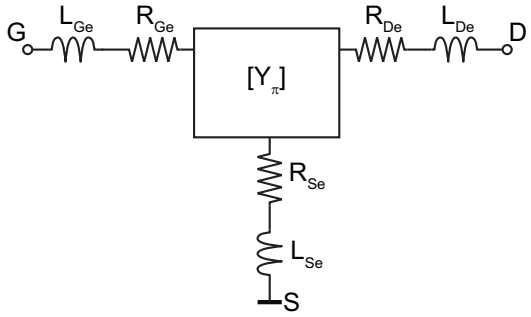

Figure 7.5: Extrinsic series resistances and inductances.

Access Parameters

After calibration of a vector network analyzer (VNA), the reference planes are not defined at the beginning and the end of the MOSFET's active zone. The remaining metal connections correspond to portions of the coplanar waveguide (CPW) lines and can therefore be modeled by the equivalent parameters of a CPW line having a given length. Since the resistance of the metal line is very small in comparison to the extrinsic resistances of the MOSFET it is not considered in the extraction procedure separately. Moreover, the access inductances are not considered seperately to simplify the extraction method. Therefore, the new $Z_{\sigma\pi}$-matrix includes the contributions of the series access parameters Z_{ga} and Z_{da}.

$$Z_{\sigma\pi} = Z_{\sigma} + Y_{\pi}^{-1} \tag{7.12}$$

with

$$Z_\sigma = \begin{bmatrix} R_{Ge}+R_{Se} & R_{Se} \\ R_{Se} & R_{De}+R_{Se} \end{bmatrix} + j\omega \begin{bmatrix} L_{Ge}+L_{Se} & L_{Se} \\ L_{Se} & L_{De}+L_{Se} \end{bmatrix} + \begin{bmatrix} Z_{ga} & 0 \\ 0 & Z_{da} \end{bmatrix}$$

$$\text{or} \quad Z_\sigma = \begin{bmatrix} R_{ge}+R_{se} & R_{se} \\ R_{se} & R_{de}+R_{se} \end{bmatrix} + j\omega \begin{bmatrix} L_{ge}+L_{se} & L_{se} \\ L_{se} & L_{de}+L_{se} \end{bmatrix} \tag{7.13}$$

Fig. 7.6 shows the equivalent circuit of a device which is located between the reference planes after calibration of the VNA. Besides the admittances Y_{ga} and Y_{da} of the CPW line, the admittance Y_{gda} is introduced, which models the parasitic coupling effects between the gate and drain fingers. The measured Y_μ-matrix of the transistor in then given by:

$$Y_\mu = Y_\alpha + (Z_{\sigma\pi})^{-1} \tag{7.14}$$

with the access-matrix

$$Y_\alpha = \begin{bmatrix} Y_{ga}+Y_{gda} & -Y_{gda} \\ -Y_{gda} & Y_{da}+Y_{gda} \end{bmatrix} \tag{7.15}$$

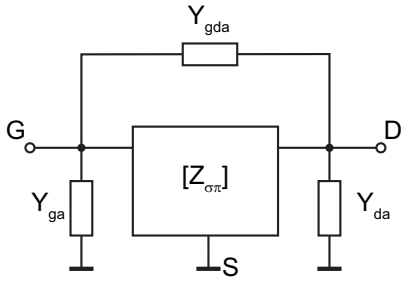

Figure 7.6: Equivalent circuit of the measured MOSFET with it's access parameters.

Finally, Fig. 7.7 presents the complete small-signal equivalent circuit for a common-source SOI MOSFET which is used for the extraction of the device parameters as described in the next section.

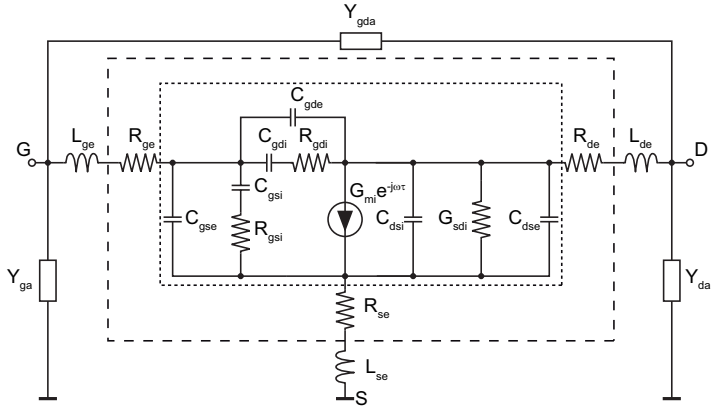

Figure 7.7: Small-signal equivalent circuit model for a common-source SOI MOSFET.

7.3 Characterization Method

For the characterization of the SB-MOSFETs, several extraction techniques are applied which rely on the conversion of S-parameters to admittance (Y) or impedance (Z) parameters (see Appendix B). The parasitic access parameters are removed in a first step, followed by the extraction of the extrinsic series resistances according to Bracale *et al.* [104]. Then, the intrinsic device parameters are extracted using the method of Raskin [101, 102].

7.3.1 De-Embedding Procedure

The first step of the extraction procedure is to remove the parasitic access parameters Y_{ga}, Y_{da} and Y_{gda} which take parasitic coupling effects into account that might exist between the reference planes defined after calibration of the VNA. This method requires that adequate open structures for each different transistor width are implemented on the SOI wafer. The Y-matrix elements after de-embedding from the measured Y_μ-matrix are given by [105]:

$$Y_{11} = Y_{\mu 11}(\text{MOSFET}) - Y_{\alpha 11}(\text{Open}) \tag{7.16}$$

$$Y_{12} = Y_{\mu 12}(\text{MOSFET}) - Y_{\alpha 12}(\text{Open}) \tag{7.17}$$

$$Y_{21} = Y_{\mu 21}(\text{MOSFET}) - Y_{\alpha 21}(\text{Open}) \tag{7.18}$$

$$Y_{22} = Y_{\mu 22}(\text{MOSFET}) - Y_{\alpha 22}(\text{Open}) \tag{7.19}$$

After the deembedding, the reference plane is moved to the dashed box in Fig. 7.7 of the extrinsic elements.

7.3.2 Extrinsic Series Resistances

The extraction of the extrinsic resistances is performed using the cold FET method proposed by Bracale *et al.* [104]. The MOSFET is biased in the inversion regime ($V_{gs} > V_T$) and at zero V_{ds}. Under these bias conditions the device is symmetric, i. e., $C_{gs} = C_{gd}$, G_m tends to zero and G_{ds} increases with V_{gs} [106, 107]. The corresponding equivalent circuit is shown in Fig. 7.8. The real parts of the Z-parameters are related to the equivalent circuit elements by:

$$Re(Z_{11} - Z_{12}) = R_{ge} - \frac{1}{4G_{ds}} \tag{7.20}$$

$$Re(Z_{12}) = R_{se} + \frac{1}{2G_{ds}} \tag{7.21}$$

$$Re(Z_{22} - Z_{12}) = R_{de} + \frac{1}{2G_{ds}} \tag{7.22}$$

with the output conductance

$$G_{ds} = \mu_{eff} \frac{W_g}{L_g} C_{ox} (V_{gs} - V_T) \tag{7.23}$$

if a constant effective mobility μ_{eff} is assumed for varying V_{gs}. Finally, the series resistances are extracted by plotting the real parts of the Z-parameters versus the inverse gate-overdrive $1/(V_{gs} - V_T)$ and linear extrapolation to zero, i. e., $1/G_{ds} \to 0$. The extraction of the extrinsic resistances moves the reference plane to the dotted box in Fig. 7.7 which represents the intrinsic elements, but also includes the extrinsic capacitances.

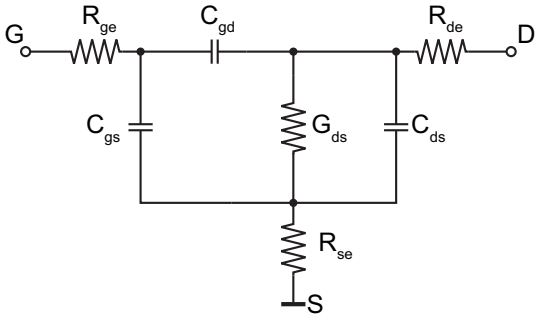

Figure 7.8: Small-signal equivalent circuit at $V_{gs} > V_T$ and $V_{ds} = 0\,\mathrm{V}$.

7.3.3 Extraction of the Capacitances and Conductances

The capacitances and conductances of the devices are then obtained using the direct extraction technique proposed by Raskin *et al.* [101, 102]. The extracted extrinsic values are used to reconstruct the matrix Z_σ which is substracted from $Z_{\sigma\pi}$ to de-embed Y_π. The following analytical expressions result in the gate-to-source C_{gs} and gate-to drain C_{gd} capacitance as well as in the intrinsic tranconductance G_{mi} and output conductance G_{dsi}:

Gate-to-Source Capacitance C_{gs}

C_{gs} is composed of an extrinsic capacitance C_{gse} and an intrinsic capacitance C_{gsi} in parallel. C_{gse} represents the overlap and fringing capacitances within the active zone.

$$C_{gs} = C_{gsi} + C_{gse} \tag{7.24}$$

with

$$C_{gse} = \frac{1}{\omega}\left[Im\left(Y_{\pi 11}\right) + Im\left(Y_{\pi 12}\right)\right] \tag{7.25}$$

extracted at $V_{gs} \ll V_T$ and $V_{ds} = 0\,\mathrm{V}$ and

$$C_{gsi} = \frac{1}{\omega}\left[Im\left(Y_{\pi 11}\right) + Im\left(Y_{\pi 12}\right) - \omega C_{gse}\right]\left[1 + \left(\frac{Re\left(Y_{\pi 11}\right) + Re\left(Y_{\pi 12}\right)}{Im\left(Y_{\pi 11}\right) + Im\left(Y_{\pi 12}\right) - \omega C_{gse}}\right)^2\right] \tag{7.26}$$

extracted from the Y_π-matrix measured at any arbitrarily chosen bias point.

Gate-to-Drain Capacitance C_{gd}

C_{gd} is composed of an extrinsic C_{gde} and an intrinsic C_{gdi} part in parallel. C_{gde} represents the overlap and fringing capacitances within the active zone.

$$C_{gd} = C_{gdi} + C_{gde} \tag{7.27}$$

with

$$C_{gde} = -\frac{1}{\omega} Im\left(Y_{\pi 12}\right) \tag{7.28}$$

extracted at $V_{gs} \ll V_T$ and $V_{ds} = 0\,\mathrm{V}$ and

$$C_{gdi} = -\frac{1}{\omega}\left[Im\left(Y_{\pi 12}\right) + \omega C_{gde}\right]\left[1 + \left(\frac{Re\left(Y_{\pi 12}\right)}{Im\left(Y_{\pi 12}\right) + \omega C_{gde}}\right)^2\right] \tag{7.29}$$

extracted from the Y_π-matrix measured at any arbitrarily chosen bias point.

Intrinsic Output Conductance G_{dsi}

$$G_{dsi} = Re(Y_{\pi 22}) + Re(Y_{\pi 12}) \tag{7.30}$$

Intrinsic Transconductance G_{mi}

$$G_{mi} = \frac{(Y_{\pi 21} - Y_{\pi 12})(1 + j\omega R_{gsi} C_{gsi})}{e^{-j\omega\tau}} \tag{7.31}$$

where τ can be neglected in short-channel devices.
Fig. 7.9 summarizes the steps of the extraction of the SSEC elements.

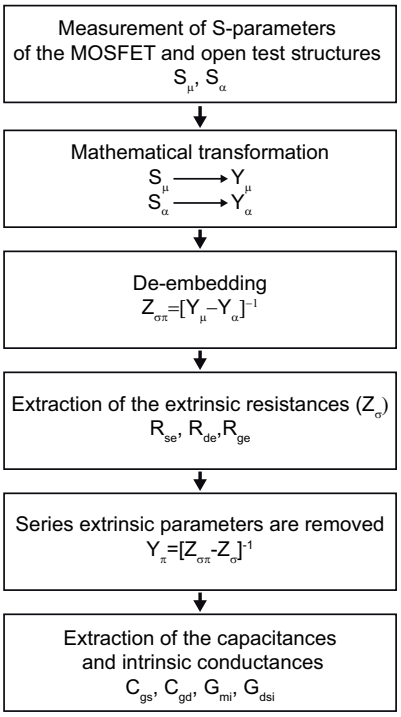

Figure 7.9: Flow-chart of the applied extraction method.

7.4 Measurement Procedure

On-Wafer *S*-parameters are measured in a wide frequency band from 40 MHz up to 40 GHz on two-finger SB-MOSFETs, presented in Chapter 5, with a total gate width of

$W_g = 2{\cdot}40\,\mu$m and $W_g = 2{\cdot}100\,\mu$m. The RF measurements are performed using an Anritsu 37369A and an HP/Agilent 8510 vector network analyzer (VNA) equipped with 100 μm-pitch ground-signal-ground (GSG) high-frequency Z-probes while the MOSFETs are DC biased using an HP semiconductor parameter analyzer. Before measuring the devices under test (DUT) an RF calibration is necessary to establish a fixed reference plane of zero phase shift, zero magnitude and known impedance at the probe tips. The array coefficients are computed by measuring a set of known devices connected at a fixed point and solving the vector difference between the modeled and measured response [75, 108]. Here, the line-reflect-reflect-match (LRRM) method is performed using a commercially available impedance standard substrate (ISS). Then, S-parameters of appropriate on-wafer open test structures are measured to de-embed the CPW pads and feed lines of the DUT's. Since the devices are fabricated on a 100 nm thick buried oxide layer, these measurements show no voltage dependence due to coupling effects through the substrate and are therefore only carried out at zero applied bias. Fig. 7.10 shows the layout of one of the open test structures which are placed close to the MOSFETs to minimize errors that might arise during the de-embedding due to process variations along the die. Measurements of different open layouts show undesired differences between S_{11} and S_{22} in case of test structures without a drain finger which is due to a strong coupling between the gate contact and the drain finger. Finally, S-parameter measurements of the SB-MOSFETs are performed under different bias conditions to facilitate the extraction of the extrinsic and intrinsic device parameters.

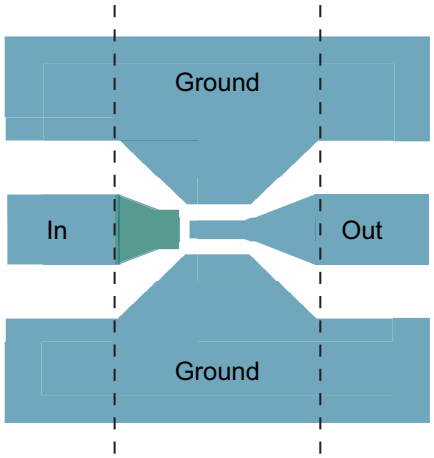

Figure 7.10: On-wafer open test structure for de-embedding of the CPW pads and feed lines. The reference planes are visualized by vertical dashed lines.

7.5 Gate-Length Dependence

7.5.1 Extrinsic Series Resistances

From the small-signal equivalent circuit, presented in Fig. 7.7, we extract the extrinsic series resistances using the cold FET extraction procedure presented in Chapter 7.3.2. Fig. 7.11 shows the source R_{se}, drain R_{de} and total S/D resistances $R_{se/de}$ of p- and n-type SB-MOSFETs with implantation doses of $3 \cdot 10^{15}$B/cm^2 and $3 \cdot 10^{15}$As/cm^2, respectively. The difference in the values of R_{se} and R_{de} is due to an asymmetry between source and drain [109] which might be related to differences in the encroachment of NiSi under the spacer. The decrease of $R_{se/de}$ with the gate length is related to Bracale's extraction method and more precisely to the assumption made by Bracale about the constant carrier mobility as a function of the applied gate-source voltage [106, 110]. This assumption is not valid for thin gate dielectrics, like the used 3.5 nm thick SiO_2, where the carrier mobility decreases with increasing gate-source voltage. The introduction of a mobility degradation factor results in an additional gate-length dependent term in Equations 7.21-7.22 [106] which shows that R_{se} and R_{de} are overestimated if only one gate-length is considered. Therefore, the S/D resistances of the SB-MOSFETs are obtained by extrapolation of the resistances to zero gate-length, where the mobility degradation does not affect the extrapolation. The S/D resistance of the n-type devices on the 20 nm-thick SOI substrate is $R_{se/de} = 718\,\Omega\mu$m, whereas a value of $R_{se/de} = 2.56\,\mathrm{k}\Omega\mu$m is evident for the p-type devices. For n-type devices $R_{se/de}$ is comparable to the value of $600\,\Omega\mu$m which is extracted from the DC characteristics for SB-MOSFETs fabricated on 30 nm thick SOI in Chapter 6.3.4 if the thickness ratio is taken into account. The higher $R_{se/de}$ of the p-type SB-MOSFETs agrees well with the DC characteristics shown in Fig. 6.20, where an exponential onset is still observed in the output characteristics, indicating a high Schottky barrier height. These devices suffered undesirably more during RIE-etching of the spacers. By optimizing the spacer etching process, where the loss of highly doped Si at the S/D regions is minimized, a similar $R_{se/de}$ for p-type SB-MOSFETs as for n-type devices is expected since dopant segregation results in Schottky barrier heights of around 0.1 eV for both, As and B segregation (see Chapter 4.8).
Currently there is no known manufacturable solution for the requested $200\,\Omega\mu$m on fully depleted SOI (cf. ITRS Roadmap [2]). Therefore, the achieved $R_{se/de}$ values seem to be very promising, especially, when the fabrication process would be even more optimized by combining dopant segregation with elevated S/D, for instance.

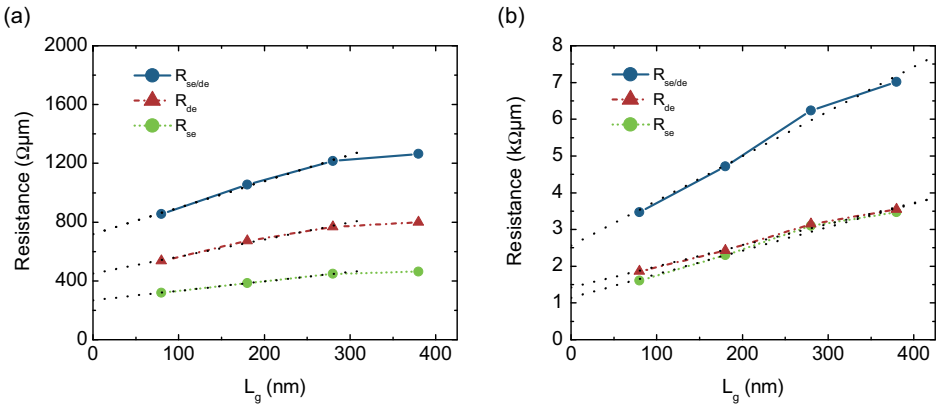

Figure 7.11: R_{se}, R_{de} and total S/D resistance $R_{se/de}$ of (a) n-type and (b) p-type SB-MOSFETs as a function of the gate length. $R_{se/de}$ of 718 $\Omega\mu$m for devices with $3 \cdot 10^{15}$As/cm^2 and 2.56 k$\Omega\mu$m for SB-MOSFETs with $3 \cdot 10^{15}$B/cm^2 are extracted.

As expected, the extracted gate resistances of the partially silicided n$^+$-poly-Si gate stacks, which are also implanted during the S/D implantation, show an increase with decreasing gate length (see Fig. 7.12(a)). Since the gate fingers are in parallel, the gate sheet resistance $R_\square$ can be calculated by:

$$R_\square = \frac{R_{ge} \cdot L_g}{W_g} \cdot 2 \qquad (\Omega/\square) \tag{7.32}$$

Sheet resistances of 4.3 $\Omega/\square$ and 2.3 $\Omega/\square$ can be calculated for the n-type and p-type devices as shown in Fig. 7.12(b). These values agree well with literature data where values of 2.2 $\Omega/\square$ are observed for boron implanted gate stacks and between 2.8 $\Omega/\square$ and 20 $\Omega/\square$ for arsenic implanted silicided gate stacks, respectively [101, 102, 111].

7.5.2 Capacitances

The parasitic capacitances strongly degrade the RF performance of MOSFETs. Consequently, their extraction in the off-state (depletion), in the on-state (inversion) and in saturation is mandatory to control and optimize the fabrication process.

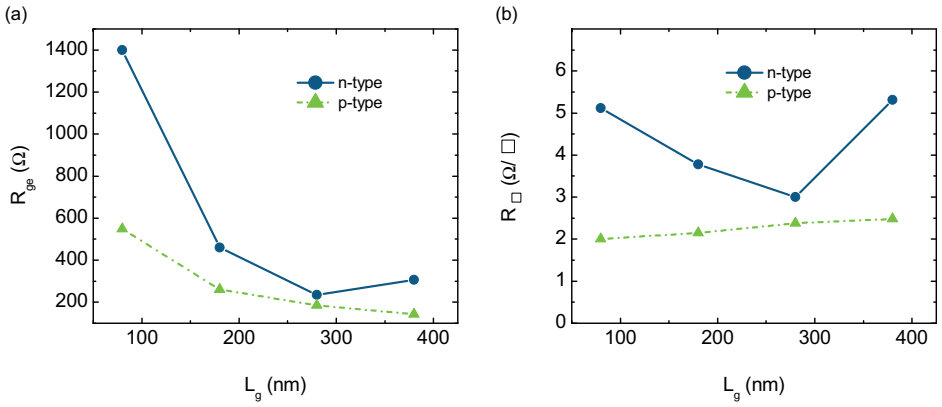

Figure 7.12: (a) Gate resistance R_{ge} and (b) sheet resistance $R_{\square}$ of the partially silicided n^+-poly-Si gate stacks.

Depletion Capacitance

Each of the gate-to-source C_{gs} and gate-to-drain capacitance C_{gd} in the off-state of a MOSFET consists of three capacitances, i. e., the fringing capacitance, the body depletion capacitance and the overlap capacitance. The latter might be the most crucial for SB-MOSFETs because of the difficult control of the encroachment of silicide under the spacer. Fig. 7.13 illustrates the capacitances of an SOI MOSFET in depletion with the three contributions to the capacitance.

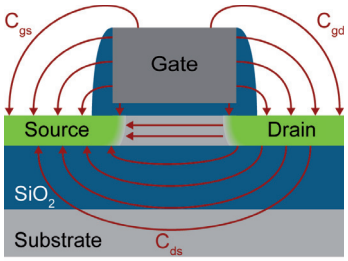

Figure 7.13: Schematic illustration of the capacitances of an SOI MOSFET in deep depletion.

In case of n-type SB-MOSFETs the depletion capacitances are extracted at $V_{gs} - V_T = $ -1 V and $V_{ds} = 0$ V, whereas a gate-source voltage of $V_{gs} - V_T = $ -0.2 V is applied for p-type devices. The normalized extracted values of C_{gs} and C_{gd} are plotted versus the gate length in Fig. 7.14. Nearly similar values of C_{gs} and C_{gd} are observed for the p-type devices which indicates a symmetric encroachment of NiSi under the spacer. The

larger difference of C_{gs} and C_{gd} for the n-type SB-MOSFETs might be due to a slight difference in the encroachment of NiSi under the spacer, resulting in varying overlap capacitances, or can also be related to a different spacer thickness of the source and drain side giving rise to different fringing capacitances.

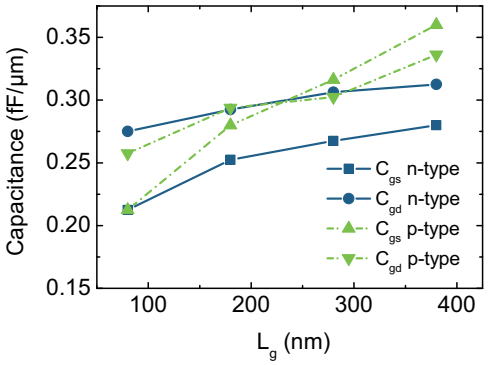

Figure 7.14: Normalized gate-to-source capacitance C_{gs} and gate-to-drain capacitance C_{gd} for n- and p-type SB-MOSFETs with different gate lengths L_g in depletion.

Inversion Capacitance

The inversion capacitances of the n-type (p-type) SB-MOSFETs are extracted at $V_{gs} - V_T = 1\,\mathrm{V}$ ($V_{gs} - V_T = $-3.2 V) and $V_{ds} = 0\,\mathrm{V}$. Fig. 7.15 shows the inversion capacitances as a function of the gate length. The capacitance decreases linearly with L_g, since $C = dQ/dV$ with Q being proportional to the device dimensions and the 3D density of states D^{3D} [112]:

$$Q \propto qt_{si}W_gL_g \int D^{3D}(E - \Phi_f^0)f(E - E_{Fs})dE \tag{7.33}$$

with Φ_f^0: potential far away from the contact interface and E_{Fs}: Fermi level at source.

Saturation Capacitance

The capacitances in saturation of the SB-MOSFETs are extracted at $V_{gs} - V_T = 0.5\,\mathrm{V}$ and $V_{ds} = 1\,\mathrm{V}$ for the n-type SB-MOSFETs and at $V_{gs} - V_T = $-2.5 V and $V_{ds} = $-1.5 V for the p-type SB-MOSFETs, respectively. The gate-to-source capacitance C_{gs} in saturation of the devices, presented in Fig. 7.16, reveals a perfectly linear scaling behavior for

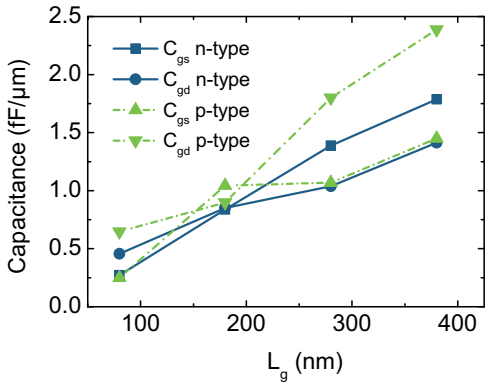

Figure 7.15: C_{gs} and C_{gd} for n- and p-type SB-MOSFETs with different gate lengths L_g in strong inversion.

p- and n-type devices with decreasing gate length [113]. It is consistent with the observations made for the inversion capacitance, where the charge in the channel depends on the device dimensions which results in a decrease of C_{gs} with the gate-length. However, for the gate-to-drain capacitance C_{gd} unexpected, non-zero values are observed. Besides the fact, that C_{gd} is strongly conditioned by the overlap capacitance caused by an overlap of the S/D silicide contacts under the gate stack and fringing fields [36, 82], a variation of C_{gd} with changing gate length can be explained by drain induced control over carriers in the channel region due to short-channel effects [114].

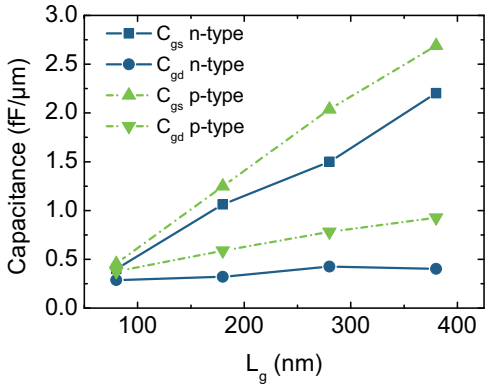

Figure 7.16: Gate-to-source capacitance C_{gs} and gate-to-drain capacitance C_{gd} for n- and p-type SB-MOSFETs with various gate lengths L_g in saturation. C_{gs} shows a perfectly linear scaling behavior.

Another interesting finding is, that the gate-to-source capacitance C_{gs} of the n-type SB-MOSFETs is close to 2/3 of the oxide capacitance C_{ox}. This confirms, that the charge control of SB-MOSFETs with a low Schottky barrier height is similar to the one of conventional MOSFETs [103]. Fig. 7.17 presents C_{gs} and $2/3\,C_{ox}$ versus gate length. The oxide capacitance is determined using split-C-V measurements on dedicated test structures and the extraction technique proposed by Romanjek *et al.* [115].

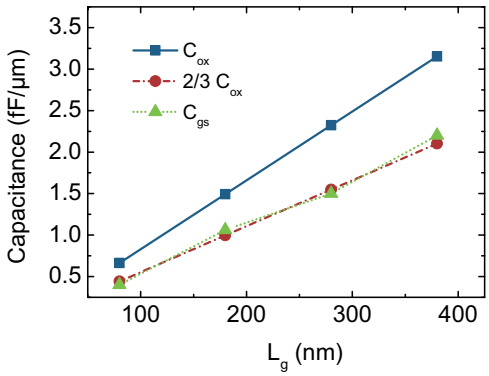

Figure 7.17: Similar to conventional MOSFETs the gate-to-source capacitance C_{gs} in saturation is close to 2/3 of the oxide capacitance C_{ox} for n-type SB-MOSFETs with low SBH.

7.5.3 Intrinsic Conductance

The intrinsic transconductance G_{mi}, the output conductance G_{dsi} and the maximum DC transconductance $G_{m,DC}$ of devices with different gate lengths in saturation are shown in Fig. 7.18. As expected, an increase of G_{mi} and G_{dsi} is observed with decreasing gate length for the n- and p-type devices. The larger difference between G_{mi} and $G_{m,DC}$ for the p-type SB-MOSFETs can be explained by much larger extrinsic series resistances due to a higher Schottky barrier of the p-type devices compared to the n-type SB-MOSFETs. The relation between the intrinsic transconductance and the DC transconductance is in a first order approximation given by the following expression:

$$G_{m,DC} = \frac{G_{mi}}{1 + G_{mi} R_{se}} \tag{7.34}$$

For instance, calculating $G_{m,DC}$ for the 180 nm-short channel SB-MOSFETs by using the extracted source resistances R_{se} from Chapter 7.5.1 results in values of 379 μS/μm for the n-type and 201 μS/μm for the p-type devices which agree very well with the measured DC transconductance $G_{m,DC}$ of Fig. 7.18. The anomalous high intrinsic

transconductance of the 80 nm p-type SB-MOSFET which is comparable to that of the n-type device might be related to an encroachment of the NiSi into the channel region and hence a shorter effective channel length.

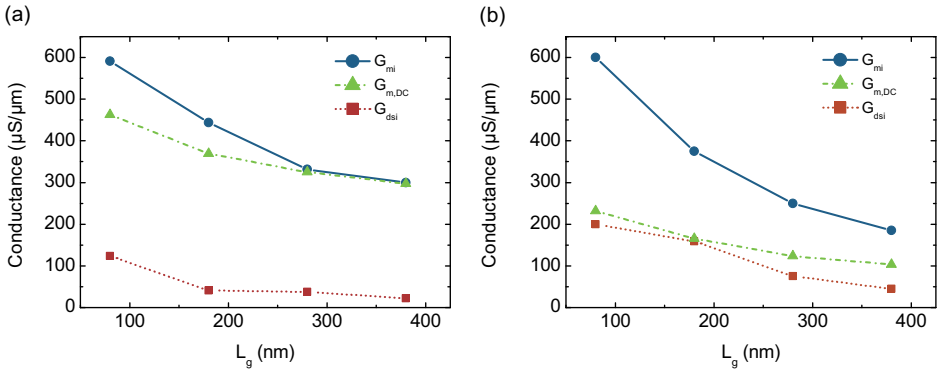

Figure 7.18: Intrinsic transconductance G_{mi}, output conductance G_{dsi} and maximum DC transconductance $G_{m,DC}$ versus gate length L_g in saturation for (a) n-type and (b) p-type SB-MOSFETs.

7.5.4 Cut-Off Frequency and Maximum Oscillation Frequency

The unity-gain cut-off frequency f_T of a transistor characterizes the point at which the current gain of the transistor vanishes, i. e., is equal to zero dB. It is therefore a measure of the high-frequency behavior of transistors and is given by [116]:

$$f_T = \frac{f_c}{\left(1 + \frac{C_{gd}}{C_{gs}}\right) + (R_{se} + R_{de})\left(\frac{C_{gd}}{C_{gs}}(G_{mi} + G_{dsi}) + G_{dsi}\right)} \tag{7.35}$$

with the intrinsic cut-off frequency

$$f_c = \frac{G_{mi}}{2\pi C_{gg}} \tag{7.36}$$

with $C_{gg} = C_{gs} + C_{gd}$, the total gate capacitance. f_c is a measure of the intrinsic ability of a MOSFET to amplify high frequency signals. Equation 7.35 shows the direct impact of the parasitic series resistances and capacitances on f_T which will be discussed in more detail in Chapter 7.9.

From S-parameter measurements, f_T is obtained from the current gain $|H_{21}| = \frac{|Y_{21}|}{|Y_{11}|}$ versus frequency plot after transformation from S- to Y-parameters and extrapolation of the linear fitted curve to 0 dB, using the theoretical slope of -20 dB/dec. Fig. 7.19

shows the cut-off frequencies of the 80 nm-short channel SB-MOSFETs. A cut-off frequency of 117 GHz is extracted for n-type SB-MOSFETs with a gate length of 80 nm at V_{gs}-V_t = 0.6 V and V_{ds} = 1.4 V where the maximum transconductance G_{mi} is obtained. The inset of Fig. 7.19(a) shows the evolution of f_T with decreasing gate lengths from L_g = 380 nm to 80 nm. For p-type SB-MOSFET with a gate length of 80 nm a cut-off frequency of 63 GHz is extracted at V_{gs}-V_t = -1.0 V and V_{ds} = -2.6 V. The high V_{ds} value needed to get the maximum f_T for the p-type device is directly related to the high extrinsic series resistance caused by a high Schottky barrier height which shifts the DC bias where the maximum transconductance G_m and therefore f_T occurs to higher V_{ds}.

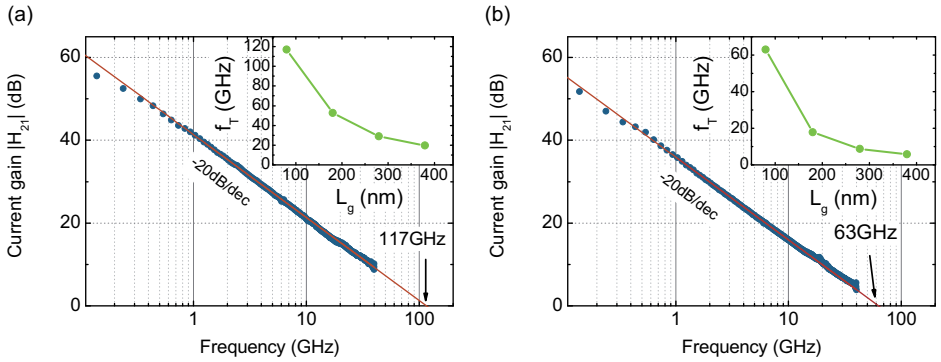

Figure 7.19: Current gain $|H_{21}|$ versus frequency plot for (a) n-type and (b) p-type SB-MOSFETs (L_g = 80 nm) showing high cut-off frequencies of 117 GHz and 63 GHz, respectively. The insets show the gate lengths dependence of f_T.

Fig. 7.20 presents a perfect $1/L_g$ dependence of f_T for decreasing gate length from 380 nm to 80 nm suggesting an impressive RF performance increase when the devices are further scaled down. This $1/L_g$ dependence of f_T is only evident for short-channel devices where velocity saturation occurs whereas a $1/{L_g}^2$ dependence is apparent for long-channel MOSFETs [40, 101, 103].

Another important figure-of-merit for microwave performance is the maximum oscillation frequency f_{max} at which the unilateral gain (ULG) becomes unity, i. e., 0 dB. ULG is defined as the maximum available gain when a lossless feedback is used to cancel the transmission of power from the output to the input [103, 117]. The maximum oscillation frequency is then given by [116]:

$$f_{max} = \frac{f_c}{2 \cdot \left(1 + \frac{C_{gd}}{C_{gs}}\right) \sqrt{G_{dsi}\left(R_{ge} + R_{se}\right) + \frac{1}{2}\frac{C_{gd}}{C_{gs}}\left(R_{se}G_{mi} + \frac{C_{gd}}{C_{gs}}\right)}} \tag{7.37}$$

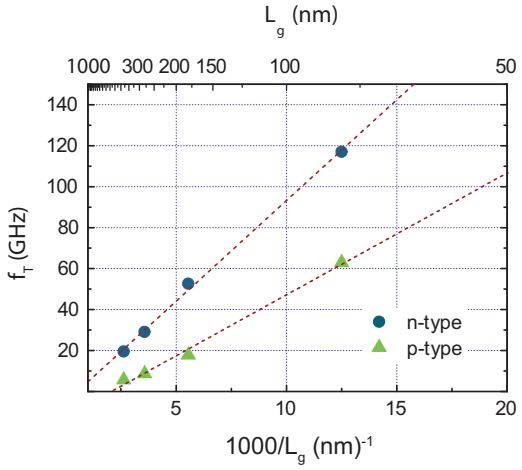

Figure 7.20: Linear dependence of f_T versus $1000/L_g$ for n-type and p-type SB-MOSFETs indicates an impressive RF performance for further downscaling.

In contrast to the cut-off frequency, f_{max} also depends on the gate resistance R_{ge}. Since the measured SB-MOSFETs only consist of two gate fingers with a large gate width of $W_g = 2{\cdot}40\,\mu$m and therefore relatively large gate resistances R_{ge} (see Chapter 7.5.1) high values of the maximum oscillation frequency are not expected here. Fig. 7.21 presents f_{max} versus the gate length for the n-type and p-type SB-MOSFETs. Maximum values of 14 GHz and 11 GHz are achieved for n- and p-type devices, respectively.

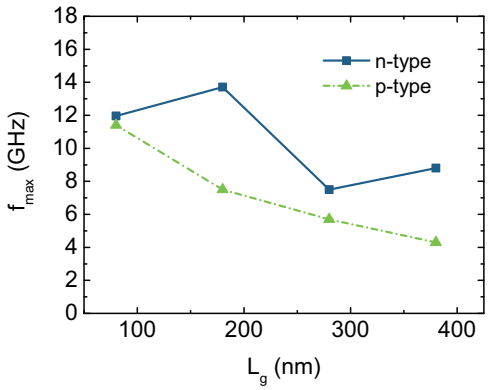

Figure 7.21: Maximum oscillation frequency f_{max} for various gate lengths for n-type and p-type SB-MOSFETs.

7.5.5 Experiment vs. Calculation

Finally, the good match between the measured S-parameter curves and the calculations based on the extracted parameters from 40 MHz up to 20 GHz are shown for 80 nm-short channel SB-MOSFETs in the Smith charts in Fig. 7.22 and Fig. 7.23. This means that the model is appropriate to fully desribe the RF characteristics of SB-MOSFETs. The Smith chart is essentially a mapping between the impedance Z plane and the reflection coefficient or $\Gamma = (Z-1)/(Z+1)$ plane. Impedances with positive real parts map inside the unit radius circle on the Smith chart whereas impedances with negative real parts map outside this circle. Moreover, impedances with positive real parts and inductive reactance map in the upper half of the Smith chart in contrast to those with capacitive reactance which map into the lower half.

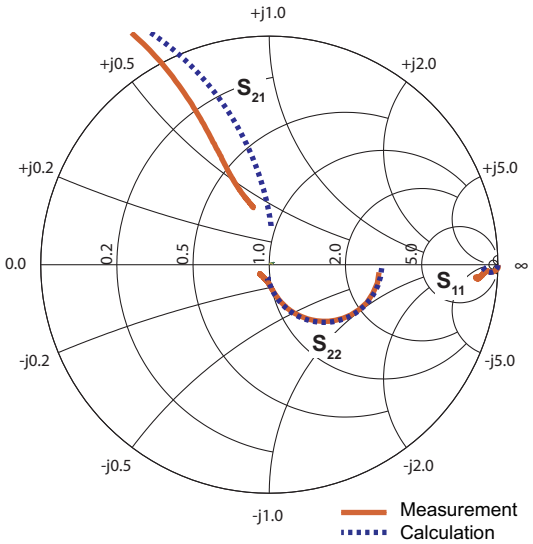

Figure 7.22: Measured and calculated S-parameters from 40 MHz up to 20 GHz for an n-type SB-MOSFET with $W_g = 2{\cdot}40\,\mu$m and $L_g = 80$ nm in saturation. The extracted parameters are: $R_{ge} = 1400\,\Omega$, $R_{se} = 320\,\Omega\mu$m, $R_{de} = 536\,\Omega\mu$m, $C_{gs} = 0.4\,$fF$/\mu$m, $C_{gd} = 0.29\,$fF$/\mu$m, $G_{mi} = 591\,\mu$S$/\mu$m, $G_{dsi} = 124\,\mu$S$/\mu$m.

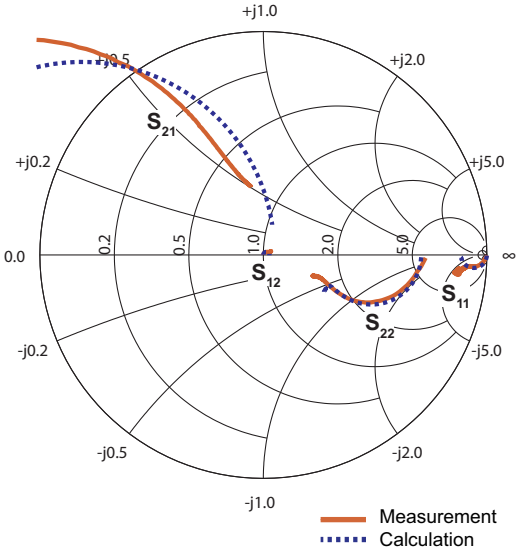

Figure 7.23: Measured and calculated S-parameters from 40 MHz up to 20 GHz for a p-type SB-MOSFET with $W_g = 2{\cdot}40\,\mu$m and $L_g = 80$ nm in saturation. The extracted parameters are: $R_{ge} = 548\,\Omega$, $R_{se} = 1603\,\Omega\mu$m, $R_{de} = 1864\,\Omega\mu$m, $C_{gs} = 0.46\,\text{fF}/\mu$m, $C_{gd} = 0.38\,\text{fF}/\mu$m, $G_{mi} = 600\,\mu\text{S}/\mu$m, $G_{dsi} = 200\,\mu\text{S}/\mu$m.

7.6 Gate-Width Dependence

To study the impact of the gate width on the RF performance, SB-MOSFETs with $W_g = 2{\cdot}40\,\mu$m and $W_g = 2{\cdot}100\,\mu$m are investigated. Fig. 7.24 shows the extracted parameters for both gate widths and two gate lengths. Whereas R_{ge} increases proportional to W_g/L_g an inversely proportionality between R_{se} and R_{de} to W_g is observed in Fig. 7.24(a). The conductances G_{mi} and G_{dsi}, presented in Fig. 7.24(b), are found to be proportional to W_g/L_g in contrast to the capacitances C_{gs} and C_{gd}, see Fig. 7.24(d), which scale with $W_g L_g$. In summary, the SB-MOSFETs follow linearily the expected scaling rules.

Fig. 7.25 shows the variation of f_T and f_{max} for the two different gate widths. Contrary to f_{max}, the cut-off frequency does not change with W_g. This can be explained by comparing Equation 7.35 and 7.37 where no dependence on R_{ge} is observed for f_T in contrast to f_{max}. Moreover, the gate widths dependence cancels completely out since G_{mi} and G_{dsi} are proportional to W_g/L_g, C_{gs} and C_{gd} to $W_g L_g$ and R_{se} and R_{de} to $1/W_g$.

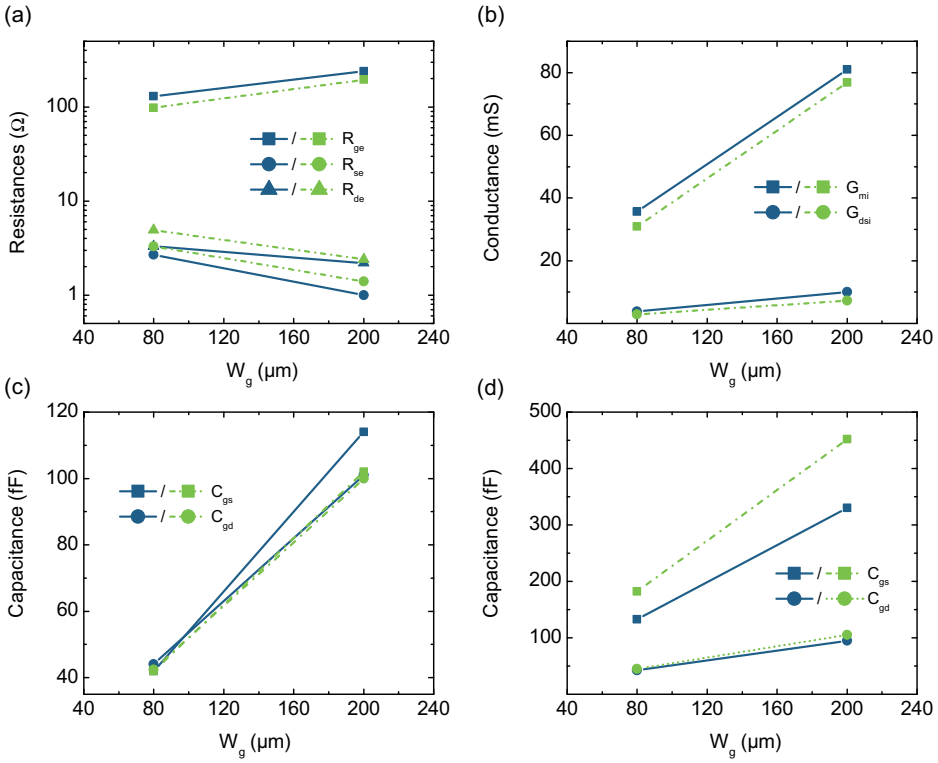

Figure 7.24: (a) Extrinsic Resistances R_{ge}, R_{se} and R_{de}, (b) conductances G_{mi} and G_{dsi} and (c) capacitances C_{gs} and C_{gd} in depletion and (d) in saturation for SB-MOSFETs with two different gate lengths of $L_g = 280\,\text{nm}$ (blue solid line) and $L_g = 380\,\text{nm}$ (green dotted line).

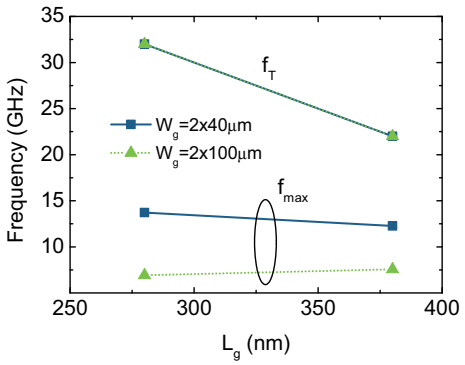

Figure 7.25: Cut-off frequency and maximum oscillation frequency for SB-MOSFETs with two different gate widths.

7.7 SB-MOSFET with an Optimized Process Flow

With the knowledge of the extracted parameters presented in Chapter 7.5, n-type SB-MOSFETs with thinner SiO_2 gate spacers and an optimized spacer etching process are fabricated. These process changes should result in a better control of the NiSi encroachment under the spacer and lower S/D resistances. Moreover, the SB-MOSFETs are fabricated using different As implantation doses to study for the first time experimentally the impact of dopant segregation on the RF performance. The key device parameters are extracted from the S-parameter measurements in the same way as presented before, except for the extraction of the capacitances and the transconductance, where the pad admittances are not removed.

7.7.1 Extrinsic Series Resistances

The extrinsic series resistances of SB-MOSFETs on 20 nm thick SOI with the optimized process flow are extraced using cold FET measurements and applying the extraction procedure as described in Chapter 7.3.2 and 7.5.1. Fig. 7.26 shows R_{se}, R_{de} and $R_{se/de}$ versus the implantation dose. A strong decrease of the S/D resistance from 5.2 k$\Omega\mu$m to approximately 508 $\Omega\mu$m is observed with increasing As implantation dose which is consistent with the effectively lowered SBH (Chapter 4.9). Interesting to note is,

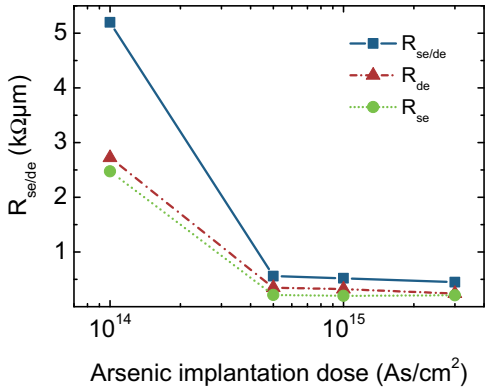

Figure 7.26: R_{se}, R_{de} and total S/D resistance $R_{se/de}$ of 180 nm-short channel n-type SB-MOSFETs as a function of the implantation dose. $R_{se/de}$ decreases from 5.2 k$\Omega\mu$m to 560 $\Omega\mu$m with increasing implantation dose.

that even at a low implantation dose of $5 \cdot 10^{14}$As/cm^2 a low $R_{se/de}$ of 560 $\Omega\mu$m is observed. In comparison to Chapter 7.5 where the minimum $R_{se/de}$ is 718 $\Omega\mu$m, a lower

S/D resistance is obtained on the same 20 nm thick SOI substrate due to the improved spacer etching process with a much better selectivity between SiO_2 and Si and therefore nearly no loss of highly doped Si at the S/D regions.

7.7.2 Dose-Dependence of the RF Performance

Fig. 7.27 presents the unity-gain cut-off frequencies f_T and the saturation currents I_{on} (V_{gs}-$V_T = 1.5\,\mathrm{V}$, $V_{ds} = 1.5\,\mathrm{V}$) of the 180 nm-short channel devices. I_{on} increases from 380 μA/μm for the lowest As dose and saturates at 720 μA/μm for higher implantation doses which is expected because of similar S/D resistances for higher doses. Although, the DC current I_{on} varies by a factor of approximately two, a change of only 20% is evident for f_T which increases from 47 GHz to 56 GHz with increasing dose.

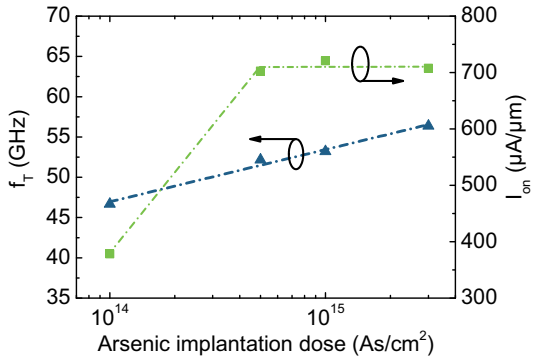

Figure 7.27: Unity-gain cut-off frequency f_T and saturation current I_{on} (V_{gs}-$V_T = 1.5\,\mathrm{V}$, $V_{ds} = 1.5\,\mathrm{V}$) of the 180 nm-short channel devices versus As implantation dose. Whereas I_{on} changes by a factor of approximately two between the lowest and the highest dose, a change of 20% is apparent in f_T.

The reason for this is that the improved carrier injection through the Schottky barrier at the source side simultaneously impacts the extrinsic transconductance G_{me} and the charge in the channel which strongly depends on the tunneling probability of carriers through the source side Schottky barrier. The channel capacitance $C = dQ/dV$ is influenced in two ways: first only carriers with high energies relative to the conduction band, where the density of states is low, are injected into the channel in case of a high Schottky barrier, and second, the tunneling probability can be significantly smaller than unity [112]. Fig. 7.28 shows the extrinsic transconductance G_{me} and the extrinsic gate-to-source C_{gse}, gate-to-drain C_{gde} and the total channel capacitance $C_{gge} = C_{gse} + C_{gde}$ which are extracted for the same 180 nm-short channel devices in saturation ($V_{ds} > V_{gs}$)

at maximum G_{me} of the SB-MOSFETs. The transconductance G_{me} increases with the implantation dose as well as C_{gse} and C_{gge}, whereas C_{gde} remains constant at a value of 0.25 fF/μm. The non-zero value of C_{gde} is due to overlap and fringing capacitances as well as DIBL [114]. The increase of G_{me} with the As implantation dose can be explained by an improvement of the gate control over drive current modulation with decreasing effective Schottky barrier height. At the same time, the tunneling probability of carriers through the lower effective Schottky barrier height is significantly enhanced, resulting in an increased amount of charge injected into the channel. Therefore, we observe a higher value of C_{gge}. Since the cut-off frequency can be expressed as $f_T = G_{me}/(2\pi C_{gge})$ it varies only slightly for different As implantation doses due to the similar dependence of G_{me} and C_{gge} on the barrier height. As a result, although the Schottky barrier strongly deteriorates the DC performance, it has only little impact on the RF performance of SB-MOSFETs. This is an important finding since the presence of the tunneling barrier is often suspected to result in larger variability of SB-MOSFETs compared to conventional devices. Another important finding is that

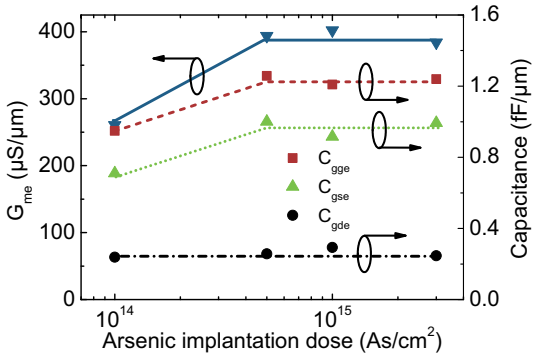

Figure 7.28: The maximum extrinsic transconductance G_{me} as well as C_{gse} and C_{gge} in saturation reveal smaller values for devices with a low implantation dose than for SB-MOSFETs with higher dose because of the high Schottky barrier at the source side ($L_g = 180$ nm). With high As dose the ratio between G_{me}/C_{gge} becomes constant.

the maximum transconductance and therefore f_T are achieved at lower bias conditions for higher implantation doses. Whereas $V_{gs} = 0.88$ V and $V_{ds} = 2.5$ V have to be applied for the lowest implantation dose in order to get f_T, lower values of $V_{gs} = 0.5$ V and $V_{ds} = 1.5$ V are needed for higher implantation doses. The corresponding DC power consumption is reduced by 27% from 705 μW/μm to 515 μW/μm. This very low DC current drive makes the SB-MOSFETs with low Schottky barrier heights suitable to address low voltage analogue applications [118].

7.7.3 Optimized 80 nm n-type SB-MOSFET

The optimized 80 nm-short channel n-type SB-MOSFETs with lower S/D resistances show a DC transconductance of 510 μS/μm. The unity-gain cut-off frequency f_T of these SB-MOSFETs is extrapolated from the current gain $|H_{21}|$ versus frequency plot using the theoretical slope of -20 dB/dec (Fig. 7.29). A cut-off frequency f_T of 140 GHz is extracted at V_{gs}-$V_T = 0.38$ V and $V_{ds} = 1.6$ V, which is the highest value reported for n-type SB-MOSFETs so far.

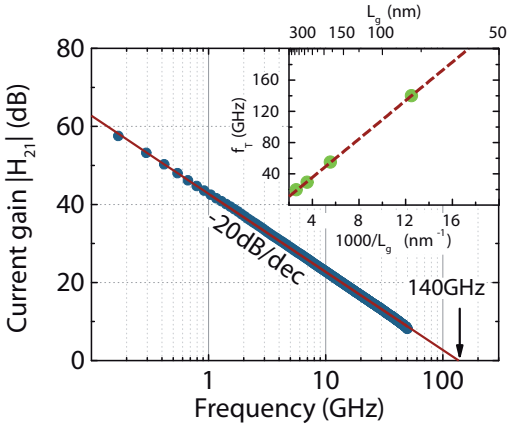

Figure 7.29: Current gain $|H_{21}|$ versus frequency for optimized n-type SB-MOSFETs with $L_g = 80$ nm ($3{\cdot}10^{15}$ As/cm^2) showing a cut-off frequency of 140 GHz. The inset shows a promising $1/L_g$ dependence of f_T.

7.8 Comparison of state-of-the-art SB-MOSFETs

Fig. 7.30 and 7.31 show the state-of-the-art cut-off frequencies of n- and p-type MOSFETs of various research groups as a function of gate length. The present SB-MOSFETs with dopant segregation show comparable RF performance to recent MOSFETs [17, 40, 82, 119–136] down to 80 nm gate length without strained channels. A linear extrapolation of f_T to smaller gate lengths indicates the expected performance increase for further downscaling which competes very well with the record-high f_T values of strained-Si MOSFETs fabricated by IBM on SOI [135] or Intel on bulk Si [136]. In case of the p-type devices the comparison of the present SB-MOSFETs with PtSi based SB-MOSFETs on SOI [17, 133, 134] reveals similar values of the extracted f_T.

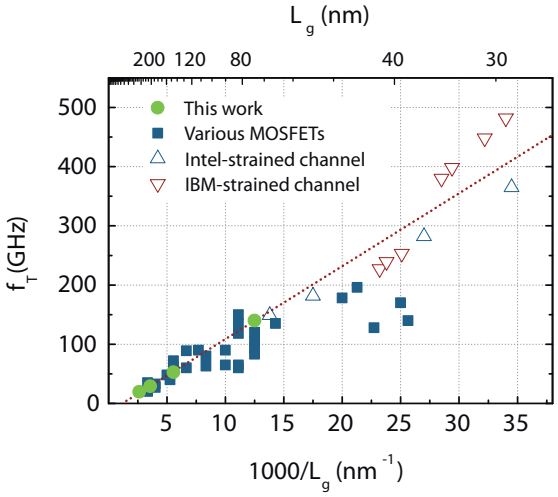

Figure 7.30: Comparision of state-of-the-art cut-off frequencies of n-type MOSFETs of various research groups in gate length dependence [40, 119–132, 135, 136]. The red dotted line shows the expected f_T for further downscaling of the present SB-MOSFETs.

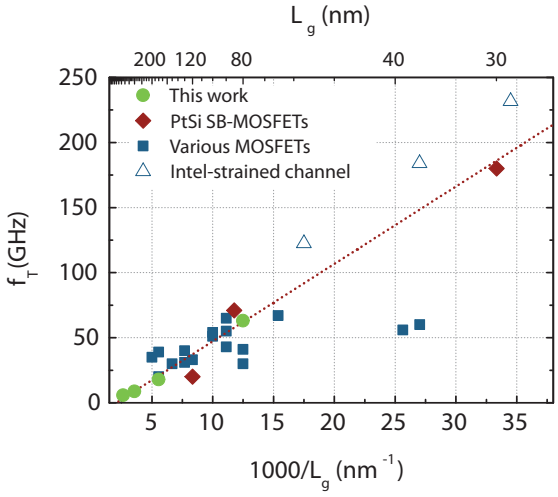

Figure 7.31: Comparision of state-of-the-art cut-off frequencies of p-type MOSFETs of various research groups in gate length dependence [17, 40, 82, 119–122, 124, 126–136]. The red dotted line shows the expected f_T for further downscaling of the present SB-MOSFETs.

7.9 Limiting Parameters

The previous sections demonstrate high-performance RF characteristics of the presented SB-MOSFETs with dopant segregation. However, the main parameters limiting the high frequency characteristics are discussed in more detail, here. Equation 7.35 and 7.37 already give some hints to identify crucial parameters. Besides minimization of the parasitic S/D resistance, which can be achieved by metal S/D with low SBH, in the optimum case, combined with elevated S/D, R_{ge} has to be minimized. Nowadays, salicide processes have enabled a remarkable reduction of the gate sheet resistance even for sub-100 nm gate length [114]. Moreover, the use of more than two gate fingers results in much lower R_{ge}. For example, the record high-performance transitors from IBM feature 48 fingers with a gate width of 2.5 μm per each finger reaching $f_{max} = 420$ GHz for n-type MOSFETs with a gate-length of 29 nm [136].

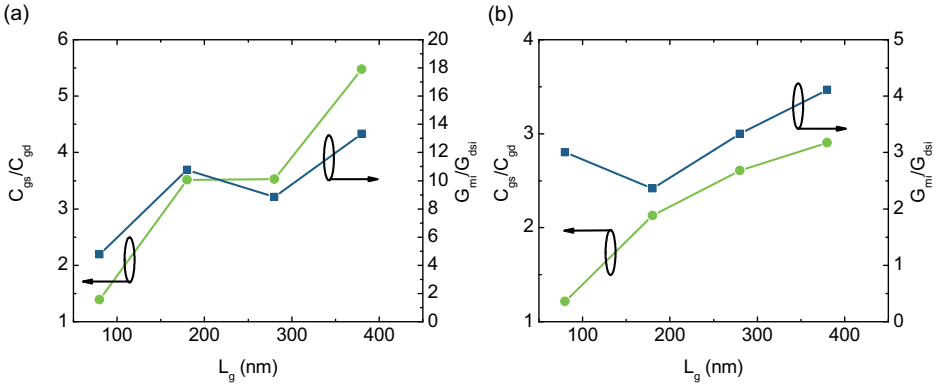

Figure 7.32: C_{gs}/C_{gd} ratio and G_{mi}/G_{dsi} ratio of (a) n-type and (b) p-type SB-MOSFETs as a function of the gate length.

Finally, the conductance ratio G_{mi}/G_{dsi} and the capacitance ratio C_{gs}/C_{gd} contribute to the degradation [114]. Fig. 7.32 shows both quantities for n-type and p-type SB-MOSFETs as a function of the gate length. The decrease of G_{mi}/G_{dsi} with the gate length is a well known short-channel effect which results in lower voltage gain for analogue applications. The observed decrease of C_{gs}/C_{gd} with decreasing gate lengths can be explained by two facts. On the one hand, C_{gs} decreases with the gate length as discussed before and on the other hand, C_{gd} increases with shorter gate lengths due to increased SCE, namely DIBL (see Chapter 2.5.2). Therefore, a reduction of SCE is mandatory to further improve the RF performance of the devices. More precisely, a smaller screening length λ is needed, which can be obtained by using thinner SOI,

thinner gate oxides or even better high-κ gate dielectrics [137]. Moreover, new device concepts like nanowires or FinFETs which provide better electrostatics than planar devices [46] emerge as promising novel device structures to solve SCE problems. However, critical device parameters like parasitic resistances and capacitances which are arising for the new architectures will become a future challenge [138–140].

7.10 Summary

A detailed investigation of radio-frequency properties of n- and p-type NiSi S/D SB-MOSFETs with dopant segregation is presented. The extrinsic and intrinsic device parameters which are extracted from small-signal parameters in dependence of the device dimensions provide a deep physical insight into the behavior of SB-MOSFETs. A perfectly linear scaling is observed for devices with gate lengths from 380 nm down to 80 nm with cut-off frequencies of 117 GHz for n-type and 63 GHz for p-type SB-MOSFETs.
A study of the implantation dose dependence is carried out on n-type SB-MOSFETs which are fabricated using an improved process flow with less loss of highly dopded Si during spacer etching and better control of the NiSi encroachment due to thinner spacers. By this, the S/D resistance is improved by 30% and cut-off frequencies as high as 140 GHz are obtained. The RF study of dopant segregated n-type SB-MOSFETs with varying implantation doses, i. e., different Schottky barrier heights, reveals a lowering of the S/D resistances by a factor of 10 when the dose is increased from $1 \cdot 10^{14}$ As/cm^2 to $3 \cdot 10^{15}$ As/cm^2. Although, the DC characteristics are strongly improved by a factor of two in the on-current between the lowest and the highest dose, f_T increases only by 20%. This smaller impact of the Schottky barrier height on the cut-off frequency which is given by $f_T = G_{me}/(2\pi C_{gge})$ can be explained by a similar behavior of G_{me} and C_{gge} for the chosen As doses which could be revealed by the extraction of the small-signal equivalent circuit parameters.
A comparison of the present SB-MOSFETs with state-of-the-art MOSFETs shows the superior RF performance which is comparable to various devices with the same gate lengths and indicates an impressive increase of f_T for further downscaling.
Finally, RF performance limiting parameters are discussed and besides the extrinsic series resistances and overlap capacitances, short-channel effects are found to be crucial since they result in a decrease of the C_{gs}/C_{gd} ratio as well as G_{mi}/G_{dsi}.

Chapter 8

Variability

The reduction of the NiSi/Si interface roughness is a major technological challenge, especially for nanoscale devices, because it might cause large variations in device performance [18, 19]. The interface roughness, which is presented in Chapter 3.2, translates from the vertical direction in case of bulk Si to the lateral direction in fully silicided SOI with an encroachment of NiSi under the spacer as schown schematically in Fig. 8.1.

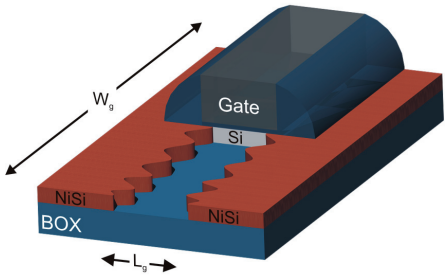

Figure 8.1: SOI SB-MOSFET showing the NiSi/Si interface roughness at the gate edge.

Since the cut-off frequency is very sensitive to device fluctuations and the S-parameter measurements allow a detailed analysis of the device parameters, this method is appropriate to study the resulting variability. Therefore, a detailed RF characterization is performed for several 80 nm-short channel SB-MOSFETs fabricated using the optimized process flow. Although, in Chapter 7.7.2 it is found, that the RF performance is not very sensitive to variations of the Schottky barrier heights while the DC characteristics are strongly degraded, we observe strong fluctuations of the cut-off frequency

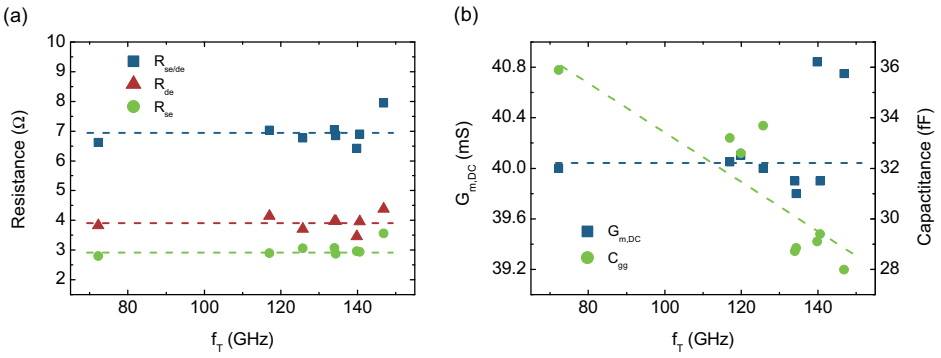

Figure 8.2: (a) Extrinsic resistances, (b) transconductance and total depletion capacitance as a function of the cut-off frequency f_T.

f_T from 70 GHz to 147 GHz for devices on the same die. To reveal the origin of these unsteadiness, several device parameters are plotted as a function of f_T in Fig. 8.2. The extrinsic resistances of all measured SB-MOSFETs show values around $R_{se/de} = 7\,\Omega$, indicating similar Schottky barrier heights. Therefore, neither the Schottky barrier height nor the transconductance $G_{m,DC}$ showing a constant value around 40 mS are the reason for the performance fluctuations. However, the extracted total gate capacitance C_{gge} in depletion shows a strong correlation with f_T. Therefore, the origin of the RF variability seems to be the depletion capacitance whose major contributions are the overlap capacitance which is strongly affected by the NiSi/Si interface roughness and the fringing capacitance.

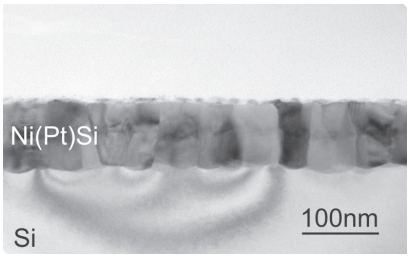

Figure 8.3: TEM image of a Ni(Pt)Si layer showing smaller grain size than NiSi.

Promising solutions to reduce the interface roughness are the incorporation of Pt in NiSi (see Fig.8.3) which results in smaller grain sizes than for NiSi [141, 142] or the use of ultra-thin epitaxial $NiSi_2$ layers [143]. Although, the use of nanowires with diameters

smaller than the grain size of NiSi seems to be advantageous, a strong drawback is the requirement of nanowire arrays to yield sufficient current flow. In these devices, the control of the NiSi encroachment into the channel region gets much more difficult and parasitic resistances as well as capacitances deteriorate the device performance.

Chapter 9

Conclusion and Outlook

Continuous downscaling of today's MOSFETs requires new innovative device concepts. In the present thesis, NiSi SB-MOSFETs with silicidation induced dopant segregation are investigated in detail using DC and RF measurements. This provides physical insights into the operation principle of these devices and more precisely into the carrier injection. The fabricated devices offer high potential for a use in ultimately scaled microelectronics.

The physical modeling of NiSi/p-Si Schottky contacts using the proposed numerical model which combines the thermionic emission theory with image-force induced barrier lowering and quantum-mechanical tunneling shows a perfect agreement between the calculated and measured data. A quantitative analysis of the enhanced carrier injection of Schottky diodes with dopant segregation using B, As or Sb reveals effective Schottky barrier heights in the 0.1 eV regime below which SB-MOSFETs are able of outperforming conventional MOSFETs. The corresponding dopant depth profiles measured by secondary ion mass spectrometry reveal the expected dose-dependent pile-up of dopants at the NiSi/Si interface which reflects the implantation dose dependence of the effective Schottky barrier height.

The steadily optimized reproducible process technology for SB-MOSFETs allows the fabrication of long- and short-channel SB-MOSFETs down to gate-lengths of 80 nm. The ground-signal-ground layout of the two-finger devices in combination with dedicated test structures is optimized for S-parameter measurements.

DC characterization of the successfully fabricated devices shows drastically improved electrical performance of SB-MOSFETs with dopant segregation when compared to SB-MOSFETs without ion implantation. Studies of the dopant dependence of the device performance indicate that the correct choice of the implantation dose in combination with the spacer thickness, i. e., the segregation length, is mandatory to achieve

superior electrical characteristics. In general, devices with higher implantation doses exhibit a distinct suppression of the ambipolar behavior and higher on-currents. The latter are result of a strong reduction of the S/D resistances for devices with high As dose which is confirmed by the extracted $R_{s/d}$ values from DC measurements.
80 nm-short channel SB-MOSFETs reveal on-currents as high as 427 μA/μm for p-type and 1150 μA/μm for n-type devices, respectively, which compete well with state-of-the-art SB-MOSFETs fabricated by TSMC, Toshiba and IEMN and highlights their outstanding performance. SB-MOSFETs fabricated on biaxially strained SOI show similar DC performance for p-type devices when compared with SOI devices. However, in case of n-type SB-MOSFETs, where a performance increase is expected due to a higher effective electron mobility, degraded performance is observed which could be a result of less segregation of As dopants or a contact problem due to abnormal oxidation of NiSi in the presence of strained silicon.
S-parameter measurements are performed for the first time on short-channel n- and p-type NiSi SB-MOSFETs with dopant segregation and facilitate the extraction of the extrinsic and intrinsic device parameters from small-signal parameters. The RF investigation of SB-MOSFETs fabricated on 20 nm thick SOI reveals a perfectly linear scaling and high cut-off frequencies f_T of 117 GHz for n-type and 63 GHz for p-type SB-MOSFETs with a gate length of 80 nm. A study of the implantation dose dependence, i. e., different Schottky barrier heights, is carried out on n-type SB-MOSFETs with an optimized fabrication process. By this, the S/D resistance is improved by 30% to 508 $\Omega\mu$m and cut-off frequencies as high as 140 GHz are obtained. The RF study of these devices with different implantation dose reveals a strongly improved on-current by a factor of two between the lowest and the highest implantation dose, due to a drastically reduced S/D resistance, while the cut-off frequency increases only by 20%. This smaller impact of the Schottky barrier height on the cut-off frequency which is proportional to G_{me}/C_{gge} can be explained by a similar behavior of the transconductance G_{me} and total gate capacitance C_{gge} for different Schottky barrier heights. A comparison of the cut-off frequencies of the present SB-MOSFETs with state-of-the-art MOSFETs shows the superior RF performance which is comparable to various devices with the same gate lengths and indicates an impressive performance increase for further downscaling. RF performance limiting parameters are identified and besides the extrinsic series resistances and overlap capacitances, short-channel effects are found to be crucial.
The RF variability of the SB-MOSFETs can be related to the depletion capacitance whose major contributions are the overlap capacitance which is strongly affected by the NiSi/Si interface roughness and the fringing capacitance.

The high potential of NiSi S/D SB-MOSFETs which is demonstrated in this work can be even improved by combination of dopant segregation with elevated source and drain. Moreover, the use of high-k gate dielectrics and thinner SOI would result in an improved electrostatic control. Furthermore, the NiSi/Si interface roughness should be reduced by using Ni(Pt)Si with smaller grain sizes or ultrathin epitaxial $NiSi_2$ which simplifies further downscaling of these devices. The integration of dopant segregation in innovative device concepts like nanowires or FinFETs which provide better electrostatics than planar devices emerge as promising device structures to minimize crucial short-channel effects. However, critical device parameters like parasitic resistances and capacitances which are arising for the new architectures will become a future challenge.

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Appendix

Appendix A

Abbreviations

BOX	buried oxide
CHF_3	trifluoromethane
CET	capacitance equivalent thickness
CMOS	complementary metal oxide semiconductor
CPW	coplanar waveguide
C-V	capacitance-voltage
DC	direct-current
DIBL	drain induced barrier lowering
DS	dopant segregation
DUT	device under test
e-beam	electron-beam
eSBH	effective Schottky barrier height
ErSi	erbium-silicide
FET	field-effect transistor
GSG	ground-signal-ground
FIB	focused ion-beam
H_2O_2	hydrogen peroxide
H_2SO_4	sulfuric acid
HBr	hydrogen bromide
HF	hydroflouric acid
HSQ	hydrogen silesquioxane
ICP	inductively coupled plasma
ITRS	International Technology Roadmap for Semiconductors
I-V	current-voltage

LPCVD	low pressure chemical vapor deposition
LRRM	line-reflect-reflect-match
MIGS	metal-induced gap states
MOS	metal-oxide-semiconductor
MOSFET	metal-oxide-semiconductor field-effect transistor
NiSi	nickel silicide
PAM	pre-allocation markers
PtSi	platinum silicide
RF	radio frequency
RIE	reactive ion etching
RMS	root mean square
RTP	rapid thermal processing
Salicide	self-aligned silicide
SB	Schottky barrier
SBH	Schottky barrier height
SCE	short-channel effects
SEM	scanning electron microscopy
SF_6	sulfur hexafluoride
SIMS	secondary ion mass spectrometry
S/D	source/drain
SOI	silicon on insulator
S-parameter	scattering parameter
SPM	sulfuric acid-hydrogen peroxide mixture
sSOI	strained silicon on insulator
STEM	scanning transmission electron microscopy
TEM	transmission electon microscopy
TEOS	tetra-ethyl-ortho-silicate
UTB	ultra-thin body
ULG	unilateral power gain
VNA	vector network analyzer
XRR	X-ray refectivity
YbSi	ytterbium silicide

Appendix B

S-Parameter Relationships

S-parameters in terms of Z-parameters	Z-parameters in terms of S-parameters
$S_{11} = \frac{(Z_{11}-1)(Z_{22}+1) - Z_{12}Z_{21}}{(Z_{11}+1)(Z_{22}+1) - Z_{12}Z_{21}}$	$Z_{11} = \frac{(1+S_{11})(1-S_{22}) + S_{12}S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}$
$S_{12} = \frac{2Z_{12}}{(Z_{11}+1)(Z_{22}+1) - Z_{12}Z_{21}}$	$Z_{12} = \frac{2S_{12}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}$
$S_{21} = \frac{2Z_{21}}{(Z_{11}+1)(Z_{22}+1) - Z_{12}Z_{21}}$	$Z_{21} = \frac{2S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}$
$S_{22} = \frac{(Z_{11}+1)(Z_{22}-1) - Z_{12}Z_{21}}{(Z_{11}+1)(Z_{22}+1) - Z_{12}Z_{21}}$	$Z_{22} = \frac{(1+S_{22})(1-S_{11}) + S_{12}S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}$

Table B.1: Relationship between S- and Z-parameters.

S-parameters in terms of Y-parameters	**Y-parameters in terms of S-parameters**
$S_{11} = \frac{(1-Y_{11})(1+Y_{22})+Y_{12}Y_{21}}{(1+Y_{11})(1+Y_{22})-Y_{12}Y_{21}}$	$Y_{11} = \frac{(1+S_{22})(1-S_{11})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$
$S_{12} = \frac{2Y_{12}}{(1+Y_{11})(1+Y_{22})-Y_{12}Y_{21}}$	$Y_{12} = \frac{-2S_{12}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$
$S_{21} = \frac{-2Y_{21}}{(1+Y_{11})(1+Y_{22})-Y_{12}Y_{21}}$	$Y_{21} = \frac{-2S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$
$S_{22} = \frac{(1+Y_{11})(1-Y_{22})+Y_{12}Y_{21}}{(1+Y_{11})(1+Y_{22})-Y_{12}Y_{21}}$	$Y_{22} = \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$

Table B.2: Relationship between S- and Y-parameters.

Appendix C

List of Publications

Proceedings and Journal Papers

C. Urban, Q. T. Zhao, C. Sandow, M. Müller, U. Breuer, S. Mantl, "Schottky barrier height modulation by arsenic dopant segregation", *Proceedings of the 9th International Conference on Ultimate Integration of Silicon, 2008. ULIS 2008, Udine*, pp. 151-154.

C. Sandow, J. Knoch, C. Urban, S. Mantl, "Improving the performance of band-to-band tunneling transistors by tuning the gate oxide and the dopant concentration", *Proceedings of the Device Research Conference 2008. DRC 2008, Santa Barbara*, pp. 79-80.

M. Müller, Q. T. Zhao, C. Urban, C. Sandow, D. Buca, S. Lenk, S. Estevez, S. Mantl, "Schottky-barrier height tuning of NiGe/n-Ge contacts using As and P segregation", *Materials Science and Engineering C*, pp. 154-155 (2008).

M. Müller, Q. T. Zhao, C. Urban, C. Sandow, U. Breuer, S. Mantl, "Schottky-barrier height tuning of Ni and Pt germanide/n-Ge contacts using dopant segregation." *Proceedings of the 9th International Conference on Solid-State and Integrated-Circuit Technology, 2008. ICSICT 2008, Beijing*, pp. 153-156.

C. Urban, C. Sandow, Q. T. Zhao, S. Mantl, "High performance Schottky barrier MOSFETs on UTB SOI." *Proceedings of the 10th International Conference Ultimate Integration of Silicon, 2009. ULIS 2009, Aachen*, pp. 65-68.

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L. Knoll, Q. T. Zhao, S. Habicht, C. Urban, B. Ghyselen, S. Mantl, "Ultra thin Ni-silicides with low contact resistance on strained and unstrained silicon." *IEEE Electron Device Letters*, Vol. 31 (2010), Issue 4, pp. 350-352.

C. Urban, M. Emam, C. Sandow, J. Knoch, Q. T. Zhao, J.-P. Raskin, S. Mantl, "Radio frequency study of dopant-segregated n-type SB-MOSFETs on thin-body SOI." *IEEE Electron Device Letters*, Vol. 31 (2010), Issue 6, pp. 537-539.

C. Urban, M. Emam, C. Sandow, Q.-T. Zhao, A. Fox, S. Mantl, J.-P. Raskin, "Small-signal analysis of high performance p- and n-type SOI SB-MOSFETs with dopant segregation." *Solid-State Electronics*, Vol. 54 (2010), pp. 877-882.

L. Knoll, Q. T. Zhao, S. Habicht, C. Urban, B. Ghyselen, S. Mantl, "Ultra thin Ni-silicides with low contact resistance on SOI and strained-SOI." *Proc. of Intern. Conf. Solid State Dev. Mat., 2009, SSDM 2009, Sendai*, pp. 390-391.

L. Knoll, Q. T. Zhao, S. Habicht, C. Urban, K. Bourdelle, S. Mantl, "Formation and characterization of ultra-thin Ni silicides on strained and unstrained silicon." *International Workshop on Junction Technology, 2010. IWJT 2010*, Shanghai, pp. 1-5.

Conference Contributions

C. Urban, Q.-T. Zhao, C. Sandow, M. Müller, S. Mantl, "Schottky barrier height modulation of NiSi/Si contacts by dopant segregation." *DPG Tagung 2008*, February 25–29th, Berlin, Germany. Oral presentation.

C. Urban, Q.-T. Zhao, C. Sandow, M. Müller, S. Mantl, "Schottky barrier height engineering of NiSi/Si contacts by dopant segregation." *Material Research Society MRS 2008*, March 24–28th., San Francisco, USA. Oral presentation.

C. Urban, Q.-T. Zhao, C. Sandow, U. Breuer, S. Mantl, "Schottky barrier height modulation by dopant segregation." *Nanoelectronic Days 2008*, May 13–16th, Aachen, Germany. Poster presentation.

C. Sandow, J. Knoch, C. Urban, S. Mantl, "Improving the performance of band-to-band tunneling transistors by tuning the gate oxide and the dopant concentration." *Device Research Conference DRC 2008*, June 23–25th, Santa Barbara, USA. Poster presentation.

C. Urban, Q.-T. Zhao, C. Sandow, M. Müller, U. Breuer, S. Mantl, "Schottky barrier height modulation by arsenic dopant segregation." *9th Conference on Ultimate Integration on Silicon ULIS 2008*, March 12–14th, Udine, Italy. Poster presentation.

C. Urban, Q. T. Zhao, C. Sandow, S. Lenk, S. Mantl, "Systematic study of SOI SB-MOSFETs with dopant segregation." *EUROSOI 2009*, January 19–21th, Gothenburg, Sweden. Oral presentation.

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S. F. Feste, C. Urban, J. Knoch, Q. T. Zhao, D. Buca, U. Breuer, S. Mantl, "Investigation of arsenic dopant segregation layers for scaled Schottky-barrier MOSFETs." *The European Material Research Society E-MRS Spring Meeting 2009*, June 08–12th, Strasbourg, France. Poster presentation.

C. Urban, M. Emam, C. Sandow, Q.-T. Zhao, A. Fox, J.-P. Raskin, S. Mantl, "High-frequency performance of dopant-segregated NiSi S/D SOI SB-MOSFETs." *39th European Solid-State Device Reasearch Conference ESSDERC 2009*, September 14–18th, Athens, Greece. Oral presentation.

L. Knoll, Q. T. Zhao, S. Habicht, C. Urban, B. Ghyselen, S. Mantl, "Ultra thin Ni-silicides with low contact resistance on SOI and strained-SOI." *Intern. Conf. Solid State Dev. Mat., 2009, SSDM 2009, Sendai*, October 7–9th, Sendai, Japan. Poster presentation.

Appendix D

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Appendix E

Curriculum Vitae

PERSONAL DETAILS

Name:	Urban
First names:	Christoph Johannes
Date of birth:	September 10th, 1979
Place of birth:	Paderborn, Germany
Nationality:	German

EDUCATION AND QUALIFICATIONS

1999	Abitur (A-level), Reismann Gymnasium Paderborn
08/1999 – 06/2000	Civilian service as paramedic, Malteser Hilfsdienst e. V.
10/2000 – 09/2005	Study of Physics at the University of Paderborn
09/2004 – 09/2005	University of Paderborn, Department of Physics, Student assistant with Prof. Dr. G. Wortmann Diploma thesis: "Magnetismus und Gitterdynamik in $SrFeO_{2.5+x}$ und verwandten Systemen: Temperatur- abängige Untersuchungen mit ^{57}Fe-Mössbauereffekt und kernresonanter Streuung von Synchrotronstrahlung"
09/2005	Diplom in Physics at the University of Paderborn
10/2005 – 01/2006	University of Paderborn, Department of Physics, Scientific employee with Prof. Dr. G. Wortmann
04/2006 – 03/2010	Research Center Jülich, Institute for Bio- and Nanosystems 1, PhD Student with Prof. Dr. S. Mantl

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   Self-Assembly and Tunneling Spectroscopy
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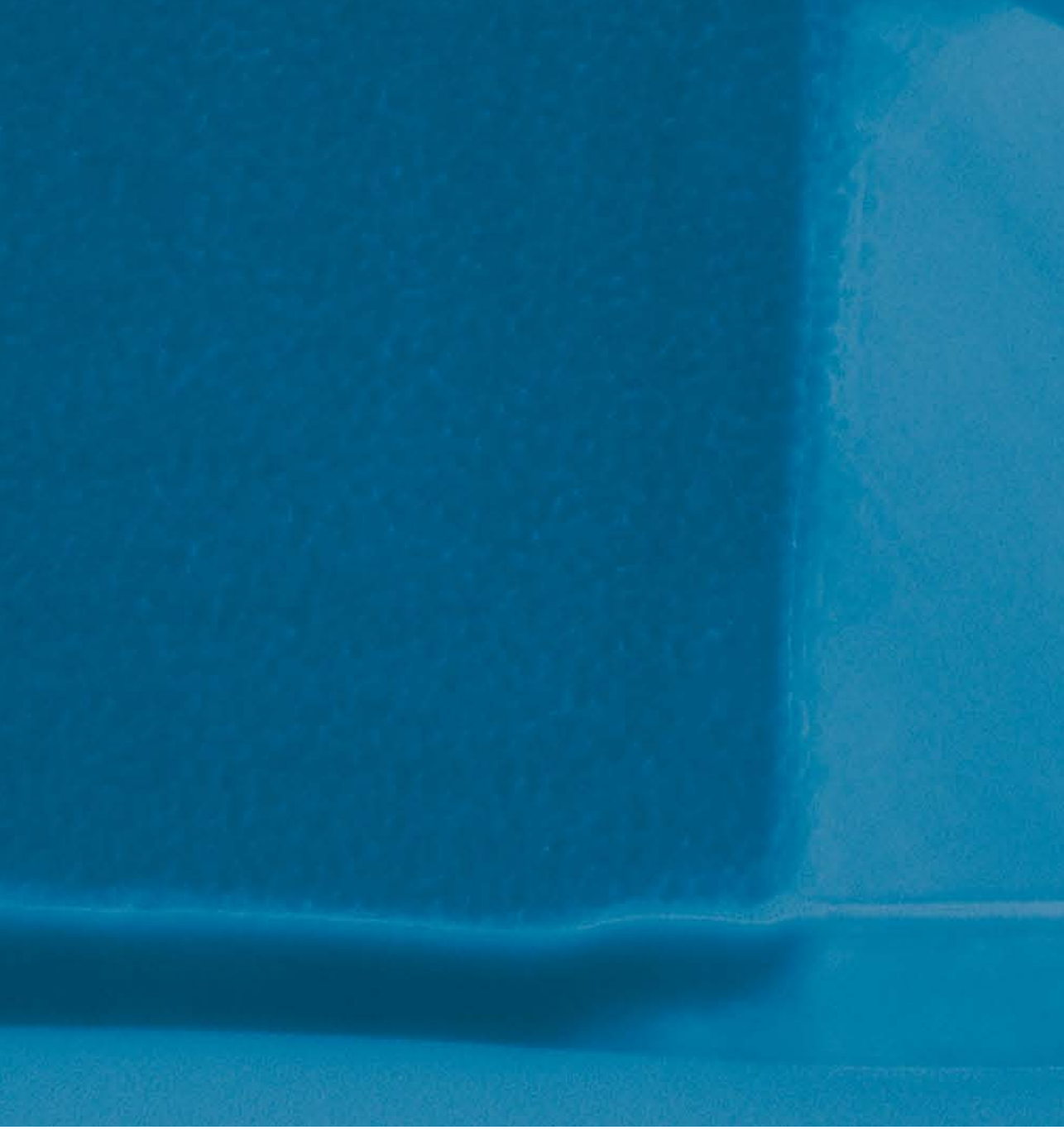

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